Miniaturized *RC* Filters Using Phase-Locked Loop

By G. S. MOSCHYTZ

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It is shown that an automatic phase-locked loop (APLL) can be used as a bandpass filter and FM discriminator while satisfying the circuit conditions imposed by microminiaturization techniques. It has the advantage over other methods of ease of adjustment and reduction in the number of circuit components. For this reason it is to be assumed that the APLL will be added to the few practical solutions of the frequency selection problem in microminiaturization available to date.

In contrast to most other applications, no assumptions can be made here about the ratio of the natural undamped system frequency to the lock range of the loop. This is taken account of in an analysis of the APLL which enables design equations and considerations to be derived. An approximation of the so-called capture ratio, defined as the ratio of capture-to-lock range, is presented. It produces results that correspond very well with the equivalent measurements.

The description of an APLL designed as RC channel filter and discriminator for a multichannel data receiver is presented. RC active circuits that are compatible with current microminiaturization techniques are employed exclusively. They are described in detail, and an analysis of the voltage-controlled oscillator used is included in the Appendix.

I. INTRODUCTION

One of the main problems in the microminiaturization of frequency-selective circuits is the considerable deterioration of Q of magnetic components when these are reduced in size to an extent comparable with other miniaturized components.[1,2,3] For the design of highly selective bandpass filters and frequency discriminators, completely new circuit design concepts that eliminate magnetic components and overcome other limitations imposed by current microminiaturization techniques must therefore be employed. At low frequencies they invariably

lead to the synthesis of narrow-band active *RC* filter circuits that are compatible with the state of the microminiaturization art. To this end a number of new circuit techniques have been described in the literature, but practical solutions to the problem are still few and not wholly satisfying.[4]

In this paper a new approach in this direction has been taken in the field of FM multiplex signal filtering by utilizing both the filtering properties of the APLL and the possibility of designing its circuits along the lines prescribed by present-day miniaturization technology. The resulting network, characterized by its simplicity, ease of adjustment and stability, shows that the APLL is a very useful filtering device in the field of circuit miniaturization. At the same time, if so desired, it also serves as a frequency discriminator.

For the purpose of introducing the APLL into the area of circuit miniaturization and to facilitate its implementation the characteristics and performance of the APLL covered in present literature are briefly reviewed. In designing the APLL for the specific function of signal filtering, the capture ratio, defined as the ratio of capture-to-lock range, has to be considered in detail. The exact capture range is given by the solution of a second-order nonlinear differential equation that is only soluble graphically by phase plane methods. To make it available in more tangible form to the circuit designer, a relatively simple yet sufficiently accurate approximation for the capture range is derived.

Design details pertinent to the realization of the APLL as an active *RC* network are given, and considerations involving the transition from discrete *RC* to thin film or integrated circuits presented. Finally, to demonstrate the effectiveness of the APLL in the field of *RC* frequency-selective circuits and to illustrate its implementation, the circuit design of an APLL employed as combined FM filter and discriminator in a multichannel data receiver operating in the audio-frequency range is described in detail. The circuits were designed to satisfy the circuit restrictions imposed by miniaturization techniques, in particular by that of tantalum thin film technology.

II. THE AUTOMATIC PHASE LOCKED LOOP

A block diagram of the automatic phase locked loop (APLL) is shown in Fig. 1. A signal corresponding to one of numerous incoming channels, which is frequency modulated about the channel center frequency ω_c, is assumed at the input. Here it is multiplied by the output of a voltage controlled oscillator (VCO) whose frequency is also centered at ω_c.

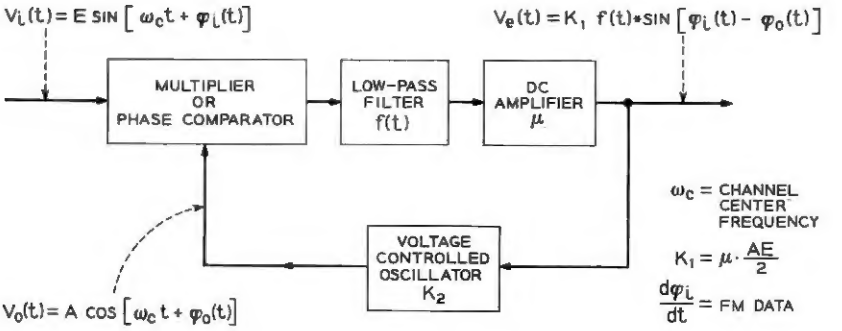

Fig. 1 — Functional block diagram of APLL.

The product is passed through a low-pass filter such that only a voltage proportional to the instantaneous phase difference, in other words to the integral of the frequency difference between the two multiplier inputs, remains. This voltage is amplified, controls the frequency of the VCO and can be considered as the output of a frequency discriminator since it is a measure of the input frequency. The multiplier serves here as a phase comparator. Furthermore it is assumed here that the frequency deviation at the input is limited to that characteristic range of steady-state frequencies within which tracking by the VCO is possible. This frequency range is called the "lock range" of the APLL, and will be discussed in more detail further on.

The frequency integration by the phase comparator results in zero error between the frequencies of the input signal and the VCO output signal in the steady state. It is maintained by a finite error voltage which is proportional to the phase difference between these two signals. This integration results in bandpass properties of the APLL with respect to noise and to interference from neighboring channels. They can be modified by the type of low-pass filter incorporated in a given loop, and are of particular significance for the application in question here.

The APLL can be designed to perform not only as a frequency demodulator but simultaneously as a selective device in the form of an FM signal separator. The extent to which either or both of these two properties is emphasized depends on the distribution and total value of the loop gain as well as on the parameters of the low-pass filter.

It will prove useful in the following discussion of APLL characteristics to apply conventional control theoretical terminology such as loop-gain, transfer function, phase margin, or cutoff frequency. The definitions

of these terms, which are somewhat unconventional, will be given as they appear in the following analysis.

2.1 *The Lock Range*

Assuming a phase comparator whose output is proportional to the sine of the error phase angle, the error voltage $v_e(t)$ after passing through the low-pass filter (see Fig. 1) is given by:

$$v_e(t) = K_1 f(t) * \sin [\varphi_i(t) - \varphi_0(t)] \tag{1}$$

where

$$K_1 = \mu(AE/2) \text{ volts}$$

and the $*$ denotes convolution. K_1 represents the sensitivity of the phase comparator multiplied by the gain μ of the amplifier, and $f(t)$ is the impulse response of the low-pass filter.

The VCO frequency ω_0 is assumed to be a linear function of the error voltage. This condition is not generally difficult to fulfill for a limited deviation ratio. With the same center frequency ω_c as that of the incoming signal, the VCO frequency is then given by:

$$\omega_0 = \omega_c + \frac{d\varphi_0}{dt}. \tag{2}$$

With K_2 in radians/(sec, volt) given as the voltage sensitivity of the VCO:

$$\omega_0 = \omega_c + K_2 v_e(t). \tag{3}$$

Substituting (1) for the error voltage and solving for the FM input signal:

$$\frac{d\varphi_i(t)}{dt} = \frac{d\varphi}{dt} + Kf(t) * \sin \varphi(t) \tag{4}$$

where

$$K = K_1 K_2 \text{ rad/sec.}$$

K is a system parameter corresponding to loop gain in conventional control theory. It equals the VCO frequency shift occurring at phase errors of $\pm \pi/2$.

For unity dc gain of the low-pass filter and an input frequency deviation from the center frequency of $\Delta\omega_i = d\varphi_i/dt$, the steady-state solution of (4) is given by:

$$\sin \varphi = \Delta\omega_i / K. \tag{5}$$

The sine of the static phase error of the APLL is therefore proportional to the input frequency deviation $\Delta\omega_i$ and inversely proportional to the gain constant K. The system locks as long as

$$| \Delta\omega_i | \leqq K. \tag{6}$$

Only within this range does (4) have a steady-state solution and a zero frequency difference $d\varphi/dt$; thus the oscillator lock range is equal to the gain constant K.

2.2 *The Capture Range*

The capture range defines the range of input frequencies to which the VCO can be synchronized when initially in the unlocked state. With an idealized low-pass filter network in the loop that rejects the high-frequency components of the phase comparator output and passes the low-frequency components unattenuated, the capture and lock ranges coincide. Modifications of this idealized case that narrow the system bandwidth with respect to the lock range can reduce the capture range appreciably.

For the application being considered here, the reduction in capture ratio (defined as the ratio of capture-to-lock range) due to narrowing of system bandwidth has to be taken into account. If, namely, the system is both to lock rapidly onto any initial frequency within the specified input frequency deviation as well as to relock rapidly after extraneous perturbations (e.g., impulse noise) might have thrown the system out of lock, the capture range has to cover the maximum frequency deviation. It is this last requirement that limits the attainable selectivity of a system all of whose parameters except those of the incorporated low-pass filter are given. However, substituting the impulse response of a generalized, or even of a simple, low-pass network in (4) and solving for the capture range is only possible by graphical phase plane methods.[5,6] The resulting second-order differential equation is nonlinear and becomes indeterminate at the values of input frequency for which the system just returns to lock. It is possible, however, to make an approximate analysis of the capture process that gives a good estimate of the capture range for a specified filter network and also some insight into the mechanism of the APLL at the time it recaptures the locked condition. The minimum attainable bandwidth compatible with a given frequency deviation thus results.

As long as the APLL is locked and in its steady state (e.g., constant

input frequency) the frequency response of the low-pass filter incorporated in the loop has no influence on the behavior of the loop. This is governed entirely by the loop gain K which defines the lock range. Out of lock, the VCO is modulated by a periodically varying signal. It therefore produces an ac error voltage at the input terminals of the low-pass filter which is subsequently attenuated according to the transfer function of the filter. This has an effect equivalent to attenuating the loop gain and with it the capture range, resulting in a capture-to-lock ratio smaller than one.

The transfer function of the low-pass filter can be expressed by

$$F(j\omega) = F_\omega e^{j\psi(\omega)} \tag{7}$$

where F_ω and $\psi(\omega)$ respectively denote the frequency and phase response. With the loop open at the VCO input terminals the error voltage for an input deviation $\Delta\omega_i$ is given by

$$v_e(t) = K_1 F_{\Delta\omega_i} \sin \Delta\omega_i t \tag{8}$$

whose peak value equals $K_1 F_{\Delta\omega_i}$. At the capture frequency $\Delta\omega_{ic}$, the corresponding peak error voltage therefore equals

$$\hat{v}_{ec} = K_1 F_{\Delta\omega_{ic}}. \tag{9}$$

By definition of the capture frequency this peak voltage is just large enough to produce the VCO frequency $\Delta\omega_{oc} = K_1 K_2 F_{\Delta\omega_{ic}}$ such that $\Delta\omega_{oc} = \Delta\omega_{ic}$ when the loop is closed. In other words, at this peak error voltage the difference frequency between input and VCO becomes zero, thus enabling the loop to go into its locked state. To do so the peak error voltage must take on its equivalent steady-state dc value

$$v_{ec} = K_1 \sin \varphi_c \tag{10}$$

which it does within the so-called "capture time" T_c. This time is in turn a function of loop parameters and initial conditions (see below). According to (5), (10) can also be written

$$v_{ec} = K_1(\Delta\omega_{ic}/K). \tag{11}$$

Equations (9) and (11) give the peak ac and steady-state dc error voltages corresponding to the unlocked and locked states respectively. Both produce the same VCO frequency $\Delta\omega_{oc}$ such that $\Delta\omega_{oc} = \Delta\omega_{ic}$. Thus both voltages must be equal, and (9) and (11) can be combined to give an approximate expression for the capture frequency $\Delta\omega_{ic}$ in

terms of filter attenuation and loop gain, namely

$$\Delta\omega_{ic} \approx KF_{\Delta\omega_{ic}}.\dagger \tag{12}$$

As is briefly explained further on, this is an approximation inasfar as the frequency $\Delta\omega_{ic}$ in the term $F_{\Delta\omega_{ic}}$ of (9) is actually not identical but somewhat smaller than $\Delta\omega_{ic}$ in (11).

For an idealized low-pass filter for which $F_\omega = 1$, (12) gives the capture range $\Delta\omega_{ic} = K$, as is to be expected. For a single low-pass filter, as shown in Fig. 2(a), the attenuation as a function of frequency is given by

$$F_\omega = 1/[1 + \omega^2 T_{co}^2]^{\frac{1}{2}} \tag{13}$$

where $T_{co} = RC$. Substituted in (12), we get

$$\frac{\Delta\omega_{ic}}{K} \approx \left[\frac{\omega_{co}}{K}\left\{1 + \frac{1}{4}\left(\frac{\omega_{co}}{K}\right)^2\right\}^{\frac{1}{2}} - \frac{1}{2}\left(\frac{\omega_{co}}{K}\right)^2\right]^{\frac{1}{2}} \tag{14}$$

where ω_{co} is the 3-db cutoff frequency of the low-pass filter and equals $1/T_{co}$.

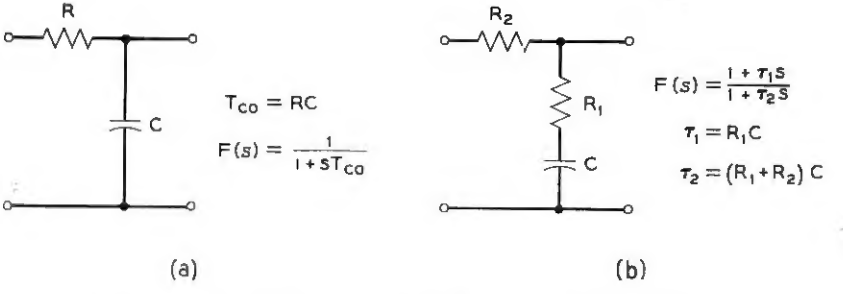

Fig. 2 — (a) Low-pass filter; (b) lag network low-pass filter.

Fig. 3 displays (14) graphically. Clearly, a simple low-pass filter in the APLL reduces the capture ratio if it attenuates frequencies within the lock range. The capture ratio decreases with the filter cutoff frequency ω_{co} and approximately equals the square root of the ratio of filter cutoff frequency to loop gain, when this ratio is small.

For a low-pass lag network as shown in Fig. 2(b), the attenuation as a function of frequency is given by

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† It was brought to the author's attention that this expression was also derived by J. A. Narud in unpublished work.

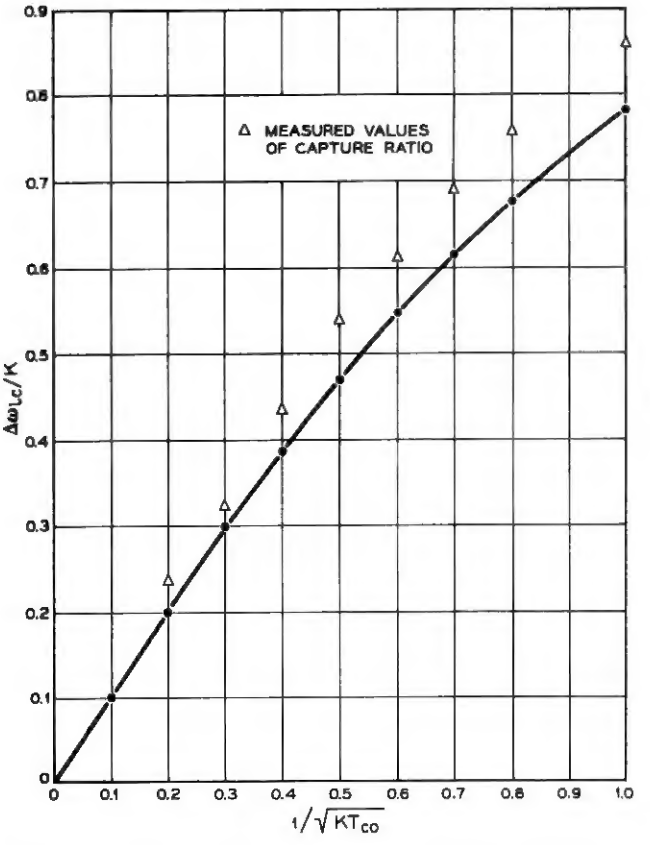

Fig. 3 — Capture range versus low-pass filter bandwidth.

$$F_\omega = \left[\frac{1 + \omega^2\tau_1^2}{1 + \omega^2\tau_2^2}\right]^{\frac{1}{2}} \tag{15}$$

where

$$\tau_1 = R_1C \tag{15a}$$

and

$$\tau_2 = (R_1 + R_2)C. \tag{15b}$$

The following substitutions may be made

$$2\zeta\frac{\omega_n}{K} = \frac{1 + K\tau_1}{K\tau_2} \tag{16}$$

$$\left(\frac{\omega_n}{K}\right)^2 = \frac{1}{K\tau_2} \tag{17}$$

where ω_n represents the undamped natural system frequency and ζ the ratio of actual to critical damping in the small-signal closed-loop transfer function of the APLL. Combining (12), (15), (16) and (17), the capture ratio as a function of filter parameters results as

$$\frac{\Delta\omega_{ic}}{K} \approx \frac{\omega_n}{K}\left[\left\{\left[2\zeta\left(\frac{\omega_n}{K} - \zeta\right)\right]^2 + 1\right\}^{\frac{1}{2}} - 2\zeta\left(\frac{\omega_n}{K} - \zeta\right)\right]^{\frac{1}{2}}. \tag{18}$$

This expression is plotted graphically as a function of ζ with the parameter ω_n/K in Fig. 4. As is to be expected, the capture ratio increases with

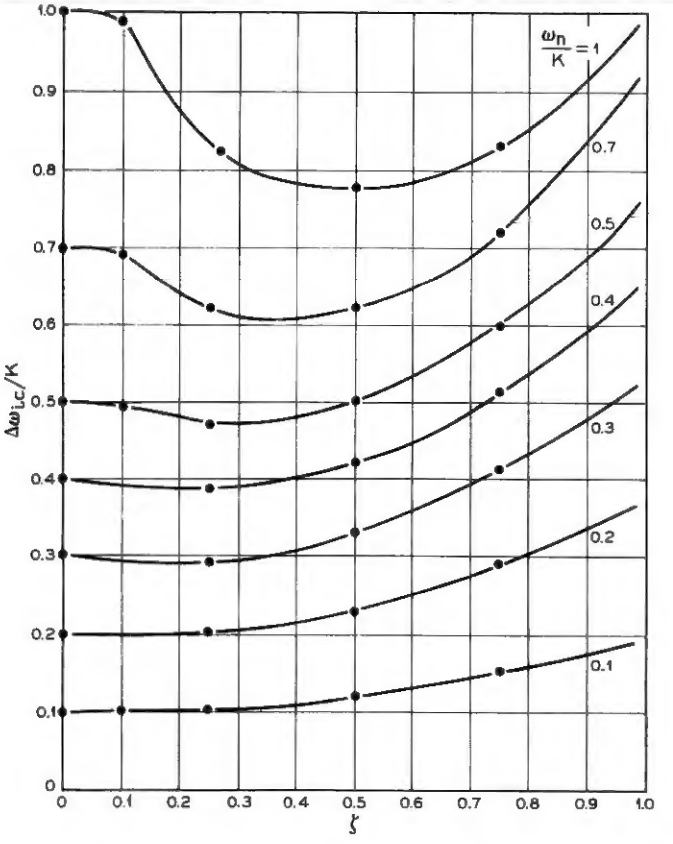

Fig. 4 — Capture range versus damping factor with parameter ω_n/K for APLL with lag network.

damping for a given system natural frequency. By making an appropriate choice of the additional parameter supplied by the lag filter, the capture ratio can now be kept closer to unity for a much smaller system bandwidth than is the case with a simple *RC* filter. In the next section the considerations that determine this choice will be discussed.

Measurements give capture ratio values that are larger than those derived from (12). The reason for this is that by equating the peak open-loop error voltage (9) with the steady state error voltage at capture (11) the assumption is made that when out-of-lock the oscillator mean frequency is equal to its rest frequency ω_c. Actually, when out-of-lock, the waveform at the phase detector output is not a pure sine wave with zero mean voltage.[7] As the VCO is frequency modulated by it, the beat frequency between input and VCO is varied, causing the rate at which the phase error characteristic (5) is traversed to vary accordingly. When the rate of traverse is slow (corresponding to a small beat frequency) the error voltage half cycle will be wider than when it is fast (large beat frequency). A net dc voltage, varying inversely with the instantaneous beat frequency, results at the phase comparator output. It causes the VCO mean frequency to leave its rest frequency by an amount $\overline{\Delta\omega_0}$ in the direction of the locked state. The exact equivalent to (12) is therefore given by

$$\Delta\omega_{ic} = KF_{\Delta\omega} \tag{19}$$

where

$$\Delta\omega = \Delta\omega_{ic} - \overline{\Delta\omega_0}\,. \tag{20}$$

As a result of (20)

$$\Delta\omega \leqq \Delta\omega_{ic} \tag{21}$$

so that

$$F_{\Delta\omega} \geqq F_{\Delta\omega_{ic}} \tag{22}$$

since F_ω is the amplitude response of a low-pass filter. Thus the actual capture range given by (19) is larger than the approximation given by (12).

Richman has shown that $\overline{\Delta\omega_0}$ can be derived for the idealized case in which $F_\omega \equiv 1$ by integrating (4) over a cycle and dividing by the period of the asynchronous loop beat frequency T_b. The results are shown qualitatively in Fig. 5. Unfortunately, as mentioned earlier (4) cannot be integrated in closed form when the impulse response of a general or even a lag network low-pass filter is substituted in the equa-

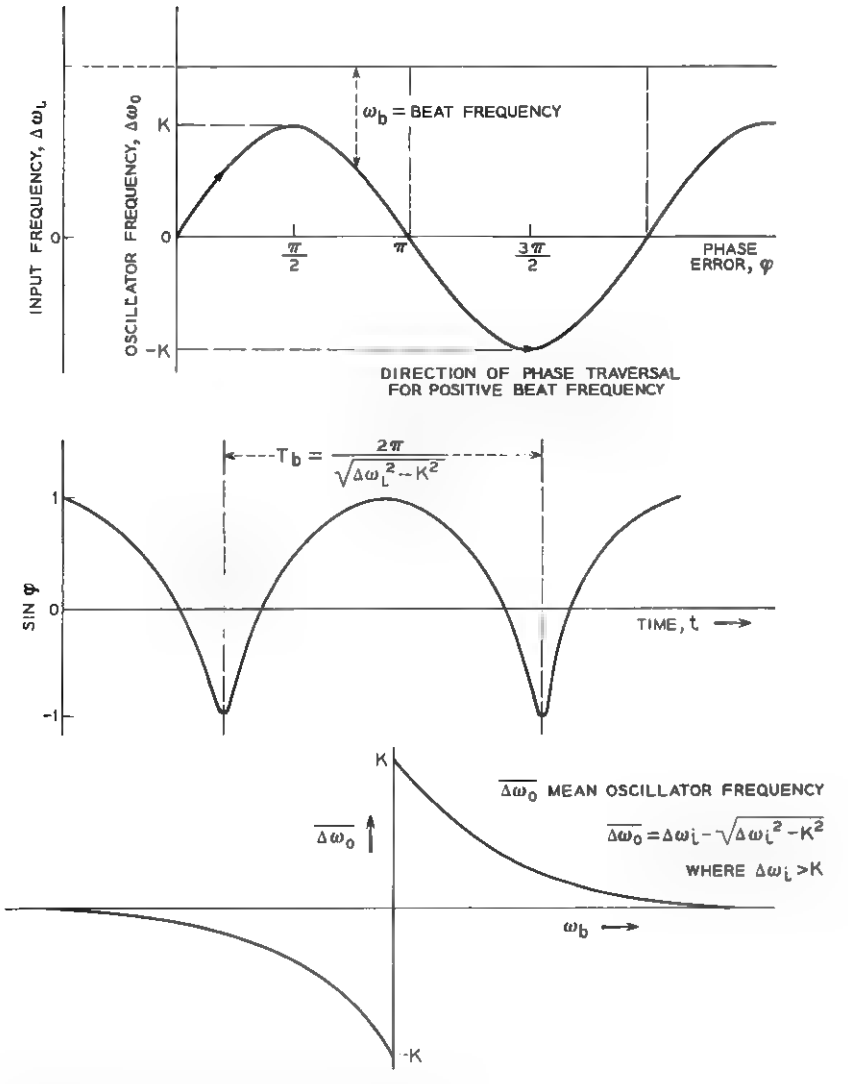

Fig. 5 — Schematic presentation of the capture mechanism for an idealized APLL without a low-pass filter incorporated in it.

tion. For this reason (19) cannot be derived analytically for anything but the idealized case.

In some circumstances, to eliminate the incompatibility of narrow bandwidth with wide capture range inherent in the APLL, the frequency-dependent control voltage mentioned above can be artificially

increased. One way of doing this is by adding a detector to the loop that is sensitive to the absolute value and polarity of the beat frequency.[8,9] Another[10] is to use a simple peak detector sensitive only to the beat frequency to disconnect the shunt elements of the low-pass filter when the loop is out-of-lock.

2.3 *Small-Signal Properties of the APLL*

Using the APLL as a frequency discriminator, the limits on phase error are set by the required system stability (lock and capture range) and by the desire to avoid distortion of the output error voltage (non-constant loop gain). To satisfy these conditions it is important to operate within the linear range of the phase comparator characteristic, e.g., within one radian phase error. Equation (4) can then be linearized and, respresenting the loop variables by their Laplace transforms (upper-case symbols), a linearized servo block diagram may be derived (see Fig. 6). The $1/s$ term takes the integration of the frequency difference by the phase comparator into account. The open-loop transfer function is given by

$$\frac{\Omega_0}{\Delta\Omega} = \frac{K_1K_2F(s)}{s} \tag{23}$$

and the closed-loop transfer function in terms of the output voltage V_e and input deviation Ω_i is given by

$$T(s) = \frac{V_e}{\Omega_i} = \frac{1}{K_2}\frac{K_1K_2F(s)}{s + K_1K_2F(s)}. \tag{24}$$

Thus the APLL has an inherent low-pass filter characteristic that is modified by the type of network $F(s)$ inserted in it. Obviously, the filter bandwidth is understood to be with respect to sinusoidal modulation of the input phase or frequency caused by noise or neighboring signal channels, and not to amplitude modulation as in conventional

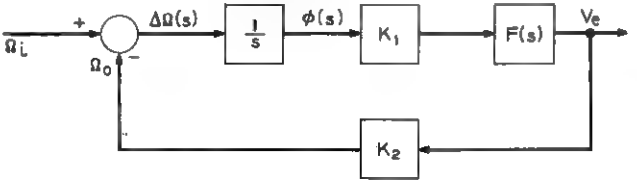

Fig. 6 — Linearized servo block diagram of APLL.

filter terminology. In this sense the APLL operates as a frequency noise or a jitter filter with respect to the input signal or signals.

The 3-db closed-loop bandwidth of the system characterized by (24) is equal to its open-loop crossover frequency or the frequency for which the open-loop gain given by (23) is equal to unity. Evaluation of this frequency results in precisely the same expression as was obtained in the capture frequency derivation given by (12). This means that an approximation for the capture range of an APLL is given by its 3-db closed-loop bandwidth.

It has been shown[11] that the mean square jitter of the VCO frequency and of the phase error caused by random interference at the input is proportional to the noise bandwidth of the system given by

$$B = \int_{-\infty}^{+\infty} | T(j\omega) |^2 \, d\omega. \tag{25}$$

This is constant for a simple RC filter (Fig. 2a), because the decrease in damping compensates for the area of the squared transfer function decreased by a reduced cutoff frequency. It can, however, be reduced by the lag network shown in Fig. 2(b), and previous papers[12,13,14] have demonstrated how the proper choice of its parameters can optimize system performance for various applications. The lag network also allows for the static phase error to be determined independently of the 3-db closed loop or of the noise bandwidth, which is important for the present application. Unfortunately, as was shown earlier, a reduction in bandwidth with respect to lock range always results in a reduced capture ratio. The ratio of capture range to noise bandwidth therefore represents a useful figure of merit that characterizes the APLL adequately for certain applications.

To calculate the noise bandwidth, (15), (16) and (17) are substituted into (25). Integrating gives

$$\frac{B}{K} = \frac{\pi}{2\zeta} \frac{\omega_n}{K} \left[1 + \left(2\zeta - \frac{\omega_n}{K} \right)^2 \right]. \tag{26}$$

Minimizing the noise bandwidth results in the following condition for the network parameters

$$\zeta_0 = \tfrac{1}{2}[1 + (\omega_n/K)^2]^{\frac{1}{2}}. \tag{27}$$

Substituting this in (26)

$$B_{\min}/K = 2\pi(\omega_n/K)^2[\{1 + (K/\omega_n)^2\}^{\frac{1}{2}} - 1] \tag{28}$$

which represents the two-sided minimum bandwidth as a function of

natural frequency and lock range, (see Fig. 7). Substituting (27) into (18) gives

$$(\Delta\omega_{ic}/K)\,|_{cpt} \approx x[\,\{[x(1+x^2)^{\frac{1}{2}} - \tfrac{1}{2}(1+x^2)]^2 + 1\}^{\frac{1}{2}} - \{x(1+x^2)^{\frac{1}{2}} - \tfrac{1}{2}(1+x^2)\}\,]^{\frac{1}{2}} \tag{29}$$

where

$$x = \omega_n/K.$$

Equation (29), plotted in Fig. 7, represents the approximate capture ratio given by (12) after the system has been optimized for minimum

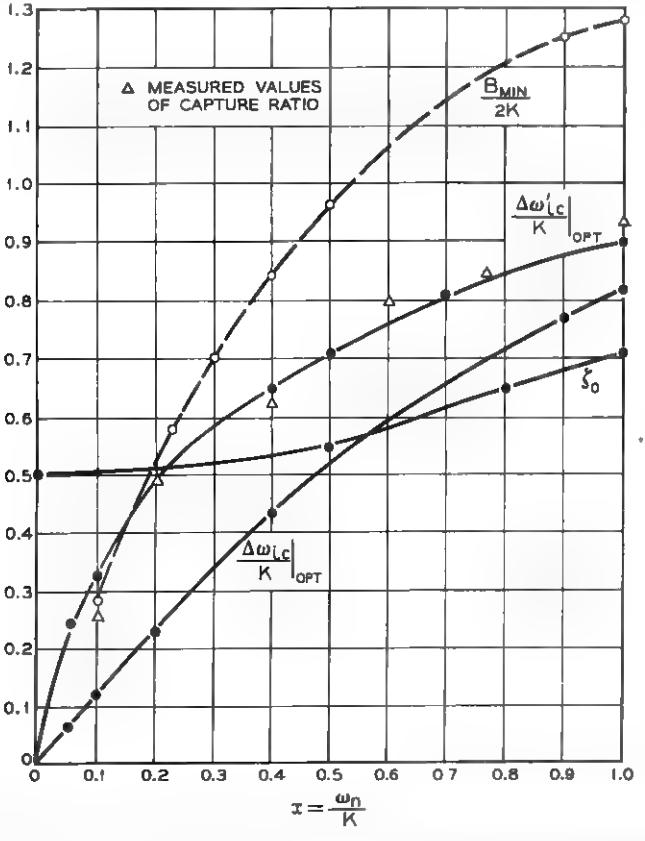

Fig. 7 — Relative noise bandwidth ($B_{min}/2K$), capture range approximations ($\Delta\omega_{ic}/K$) and ($\Delta\omega_{ic}'/K$) and damping factor ζ_0 as a function of (ω_n/K) for an APLL optimized for minimum noise bandwidth.

noise bandwidth. Simultaneously, as was pointed out earlier, it exactly defines the open-loop crossover frequency or the 3-db closed-loop bandwidth of the APLL for an optimized lag filter.

Measurements for the capture ratio of an APLL incorporating a lag filter optimized with respect to noise bandwidth were made. The results suggested that for this case a closer approximation of the capture ratio is given by the geometrical mean of the crossover frequency derived from (12) and the lock range K. Denoting this improved approximation of capture range by $\Delta\omega_{ic}'$, we get from (29)

$$(\Delta\omega_{ic}'/K)\,|_{\text{opt}} \approx [x\{\{[x(1+x^2)^{\frac{1}{2}} - \tfrac{1}{2}(1+x^2)]^2 + 1\}^{\frac{1}{2}} - \{x(1+x^2)^{\frac{1}{2}} - \tfrac{1}{2}(1+x^2)\}\}^{\frac{1}{2}}]^{\frac{1}{2}}. \tag{30}$$

This expression has also been plotted in Fig. 7.

Combining (28) with (30) to give the figure of merit F_0 for a system optimized for minimum one-sided noise bandwidth gives

$$F_0 = \frac{\text{capture range}}{\text{minimum noise bandwidth}} \approx \frac{[x\{\{[x(1+x^2)^{\frac{1}{2}} - \tfrac{1}{2}(1+x^2)]^2 + 1\}^{\frac{1}{2}} - \{x(1+x^2)^{\frac{1}{2}} - \tfrac{1}{2}(1+x^2)\}\}^{\frac{1}{2}}]^{\frac{1}{2}}}{\pi x[(1+x^2)^{\frac{1}{2}} - x]}. \tag{31}$$

This expression is plotted in Fig. 8. It can be seen that the capture range is generally smaller than the minimum noise bandwidth. For narrow noise bandwidth systems, this may make unduly high demands on the stability of the system, in particular on the VCO and, if present, on the dc amplifier. It may then be worthwhile incorporating the already mentioned additional frequency-sensitive loop or the peak detector, sensitive to the out-of-lock beat frequency at the phase detector output, to increase the capture ratio.

For the application described here, the ratio of capture range to closed loop bandwidth $\Delta\omega_{ic}'/\Delta\omega_{ic}$ designated by F is a more practical figure of merit than the conventional F_0. It is therefore also plotted in Fig. 8. The resulting curve determines the degree of stability with respect to frequency drift that is required by a given system. This can best be illustrated by the channel frequency distribution of part of an FM multiplex system shown in Fig. 9. The assumption was made there that the bandwidth of each receiving channel filter equals the total frequency deviation in that channel. The total bandwidth BW of each channel extends halfway into the guardband on either side of a channel.

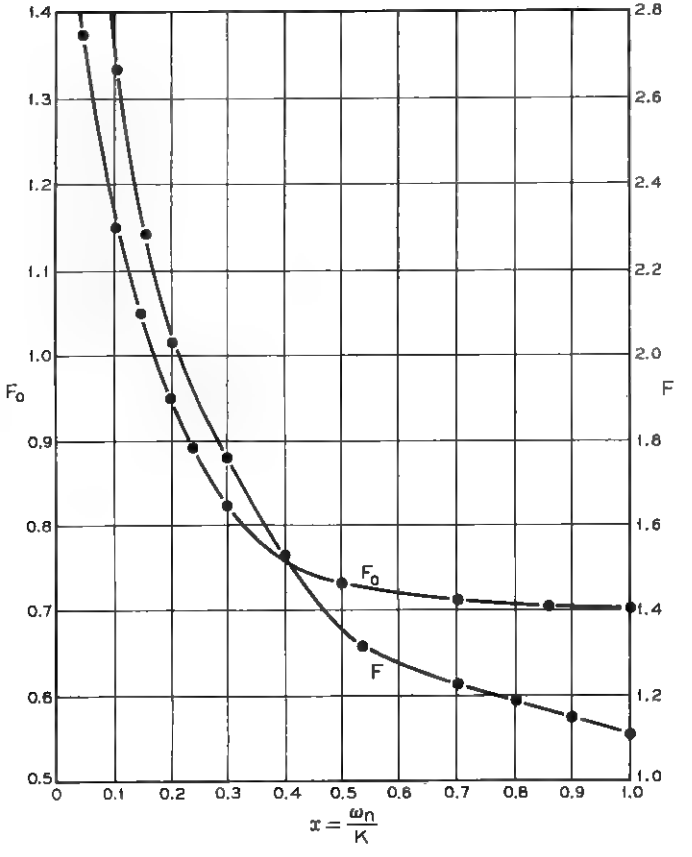

Fig. 8 — Figures of merit F_0 = capture range/noise bandwidth and F = capture range/closed loop bandwidth for minimum noise-bandwidth APLL.

Limits on the capture frequency range can then be obtained by inspection, namely

$$\text{total frequency deviation} < \text{capture range} < \text{channel bandwidth } BW. \tag{32}$$

Expressing (32) in terms of F, we get

$$1 \leqq F \leqq (BW/2\Delta\omega_{ic}). \tag{33}$$

The closer F is to its lower limit the less frequency drift may be tolerated in the receiving APLL. The more it approaches its upper limit the smaller the ratio ω_n/K must be, as Fig. 8 shows. Referring to Fig. 7, a decreasing

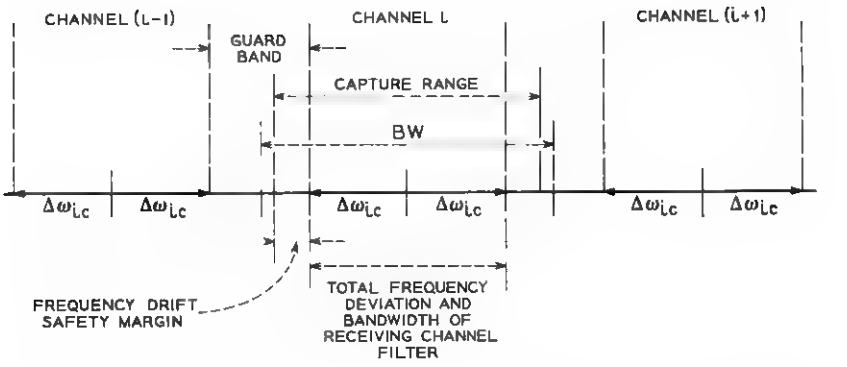

Fig. 9 – Channel frequency distribution of part of an FM multiplex system.

value of ω_n/K in turn results in a decreasing ratio $\Delta\omega_{ic}/K$. In other words, the extent by which the lock range K must exceed the closed-loop system bandwidth $\Delta\omega_{ic}$ increases as F is varied from its lower to its upper limits. Using conventional circuit techniques, the choice of F would thus be reduced to the question of whether it is more economical to attain a high degree of circuit stability or a high loop gain. Using circuit microminiaturization techniques, however, the choice depends on which of the two major approaches existing to date is taken. If integrated semiconductor circuits are to be used, low-precision components and therefore substantial frequency drift in the APLL must be expected. In this case F should be chosen as close to the upper limit given by (33) as possible. If high-stability thin film circuit components are available for design, the choice of F will be as close to the lower limit as the attainable over-all circuit stability and the lower limit on lock range allow.

The limits on lock range (or loop gain) K are determined by two different aspects of loop operation. The upper limit results directly from the upper limit on capture frequency range. With the same approximation for the capture range as that used to derive (30), namely

$$\Delta\omega_{ic}' \approx (K\Delta\omega_{ic})^{\frac{1}{2}} \tag{34}$$

and referring to Fig. 9, the upper limit on lock range in terms of channel and receiving filter bandwidth of a given system is $(BW)^2/\Delta\omega_{ic}$. It must be remembered, however, that (34) was empirically verified only with a lag network low-pass filter such as that shown in Fig. 2(b) connected in the APLL. By inspection of Fig. 9 the lower limit on lock range might be considered to equal the input frequency deviation. However,

this is true only for the case that a linear phase detector (e.g., sawtooth output) is used, since only then is loop operation linear throughout the frequency range covered at the input. With sinusoidal phase detectors which are simpler in implementation and therefore more widely used, the output is linear only to within a given percentage for phase error values that do not exceed a corresponding maximum value φ_{LIN}. Referring to Fig. 9 and (5) and (33), the limits on lock range then result as follows

$$\Delta\omega_{ic}/\sin\varphi_{\text{LIN}} \leqq K \leqq (BW)^2/\Delta\omega_{ic}\,. \tag{35}$$

Using a sinusoidal phase detector accordingly reduces the lower bound on F, thereby modifying (33) to give

$$(1/\sin\varphi_{\text{LIN}})^{\frac{1}{2}} \leqq F \leqq BW/2\Delta\omega_{ic}\,. \tag{36}$$

Besides decreasing the capture ratio, the inclusion of a low-pass filter network in the loop also increases the capture time T_c. Richman has shown[7] that for input frequencies within the capture range, this can be approximated by:

$$T_c \approx 32\Delta f_i^2/B^3 \tag{37}$$

where Δf_i is the maximum initial frequency offset and B the noise bandwidth. For many applications, the maximum frequency offset is equal to the system bandwidth. Approximating this by the noise bandwidth, the capture time is then given by

$$T_c \approx 8/\pi^2 B. \tag{38}$$

III. RC CIRCUIT DESIGN OF APLL

In this section general considerations for the design of an APLL filter and discriminator are discussed using *RC* active circuits that are compatible with microminiaturization techniques.

3.1 *The Phase Comparator*

Analog multipliers can be built[15] such that the output contains a dc term proportional to the input phase difference, but these are either complex or unsuitable for a composite input signal. Semiconductor switched modulators or phase-sensitive choppers can be used for the same purpose and are very much simpler and more economical to build. This is why they have been described quite extensively in the literature,[16-19] particularly with the advent of the epitaxial planar transistor,

which makes an excellent switch when used in the inverted mode.[20] However, since these circuits are most easily operated when driven from a transformer the methods usually described are not directly applicable here. To eliminate the transformers while retaining the isolation and performance they afford it was found that the transistors can be driven from an ac-coupled current source.

The equivalent diagram of a simple series switched modulator is shown in Fig. 10(a). A sinusoidal signal is periodically switched from the output of a voltage generator with source resistance R_S to the load R_L during the time T_0. The input signal period and the switching period both equal T, and φ is the phase angle between the two signals. Fig. 10(b) illustrates a schematic interpretation of this process, in that the input sinusoidal voltage is multiplied by a square wave of unity amplitude, period T and pulse width T_0. The dc component of the resulting output voltage is then given by

$$V_{OUT} = \frac{E}{\pi} \frac{R_L}{R_S + R_L} \sin (\pi T_0/T) \cos \varphi. \tag{39}$$

The switch S can be replaced by a transistor operating in the inverted mode to give a configuration such as that shown in Fig. 10(c). The transistor must be driven from a constant current source; therefore R_1 must be large, yet still allow the transistor to be saturated throughout the ON state. The ratio of reference to input signal level E_c/E, which should be as large as possible, determines the actual values of R_1 and R_2 in a straightforward way. To prevent emitter breakdown, a diode is connected in series with the transistor base.

With the transistor connected in the inverted mode, it is the base collector junction that is driven by the reference voltage. For this reason and to sustain saturation both the ratio R_S/R_L and R_S itself must be made as small as possible, the limits again being determined by the ratio of E_c/E. This suggests the use of an emitter follower from which to apply the input signal, as shown in Fig. 10(d). Here the variable resistor R_v is initially adjusted to cancel the offset voltage by making the voltage difference between points A and B equal to zero. The switched modulator is shown feeding into a simple dc amplifier stage T_3. If necessary, this amplifier can be increasingly stabilized by well known means, as was done in the application described in the next section. If — as is the case when operating as a phase detector — only the dc component of the switched modulator output voltage is required, the low-pass filter R,C shown in Fig. 10(d) can be added.

In the switched modulator shown in Fig. 10(d) the transistor offset

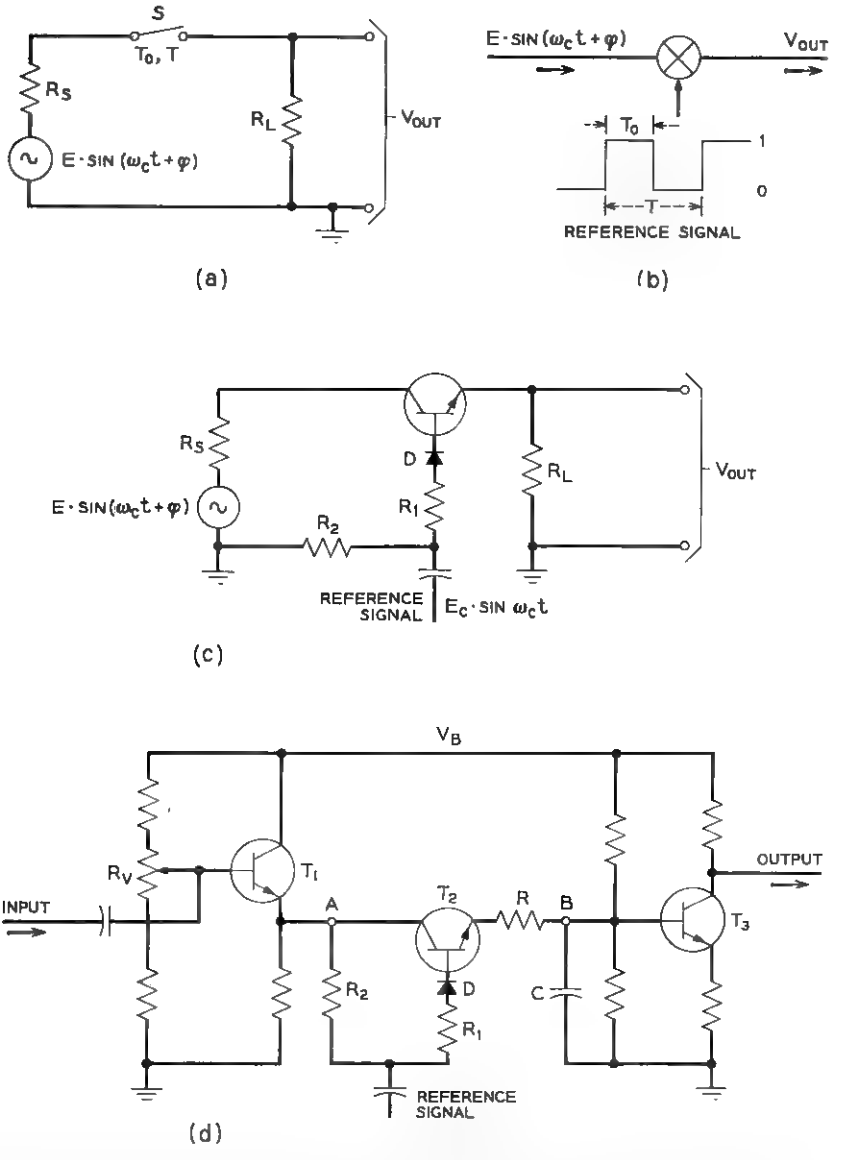

Fig. 10 — Transformerless single-transistor series-switched modulator: (a) equivalent diagram (b) functional interpretation (c) Switch S in (a) replaced by transistor in inverted mode (d) final circuit.

voltage can be entirely eliminated initially, but no compensation takes place for subsequent drift caused by temperature variations. However the circuit is operated essentially as a high-level switch, inasmuch as the input signal can be increased by more than half the reference voltage level, particularly if the latter signal is a square wave. In such cases offset voltage drift, being in the order of microvolts for silicon planar epitaxial transistors,[20] is usually negligible. For extreme stability with ambient temperature or for low-level switching applications a balanced modulator using two inverted transistors connected back-to-back gives excellent results.[16] Here again the transformer customarily driving the transistors can be replaced by a current source. Such a circuit is shown in Fig. 11 with the switching transistors driven by a high output impedance phase inverter. Offset voltages and currents can be canceled here over a wide temperature range without having to preselect or match the transistors.

Equation (39) shows that the output dc voltage of the switched modulator depends not only on the phase difference between the input and reference signals but also on the input signal amplitude. To eliminate this latter dependence an AGC circuit should precede the APLL when input level variations are anticipated.

3.2 *The Voltage-Controlled Oscillator (VCO)*

Stability of the VCO frequency is one of the main factors that determines the stability of the APLL. For a narrow filter characteristic,

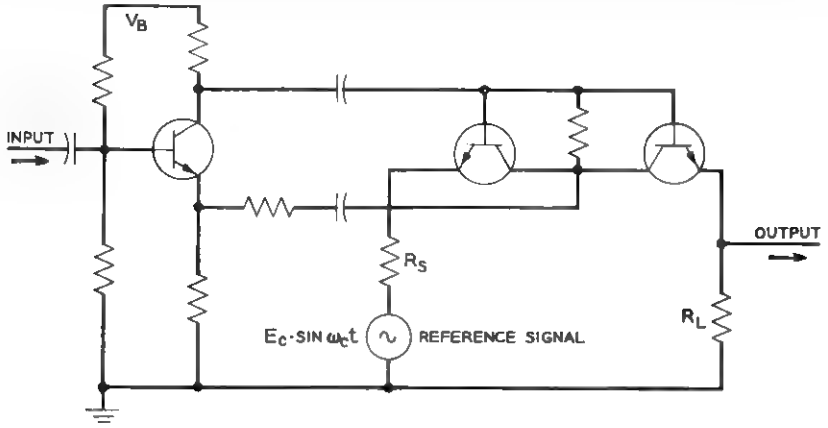

Fig. 11 — Balanced series-switched modulator fed from a phase inverter.

frequency stability with respect to temperature and power supply variations is therefore important. This can be achieved by designing the oscillator so that its frequency depends only on reliable low-tolerance passive circuit components. Highest stability can be attained with precision thin film resistors and capacitors that are matched with respect to temperature coefficients.

For circuit simplicity and economy it is desirable to minimize the number of voltage controllable elements needed to give a specified frequency deviation. Nevertheless the frequency versus control voltage must be linear for linear operation of the loop. As for the components presently available as voltage controlled elements, this depends on the frequency range of operation. Applications at high frequencies using varactors are not uncommon, whereas the mean capacitance value of these components is generally not large enough for low frequencies. In the latter case field effect transistors, varistors or diodes can be used as voltage controllable resistors over a certain range of their voltage-current characteristics.

RC oscillators suitable for frequency modulation by a control voltage can be grouped into three categories, i.e., relaxation oscillators, zero phase shift oscillators and 180° phase shift oscillators.

With relaxation oscillators, the period of oscillation is controlled by the input signal voltage. If so desired, the fundamental frequency component can be filtered out by a low-pass filter. For frequency stability, threshold compensation due to temperature variation and line voltage compensation are necessary. This entails additional regulating circuitry.

Zero phase shift voltage-controlled oscillators (i.e., Wien bridge, twin-T, bridged-T, or zero phase shift ladder network in the feedback loop) require more than one voltage-controlled element or the incorporation of some means of AGC. Changing any single element of the frequency determining network changes network loss and results in amplitude modulation.

Over a limited frequency range, amplitude variations can be eliminated in a 180° phase shift oscillator when varying only one element in the frequency determining ladder network. This is shown in Fig. 12, where attenuation and frequency curves for three and four equal-section ladder networks in which the value of a single element is varied are plotted. The ladder networks considered differ in the mode of operation (voltage or current driving source) and in the choice of variable element. In all cases the attenuation curve goes through a broad minimum rather than falling monotonically as is the case with networks used in zero phase oscillators. Experiments have verified this, in that negligible

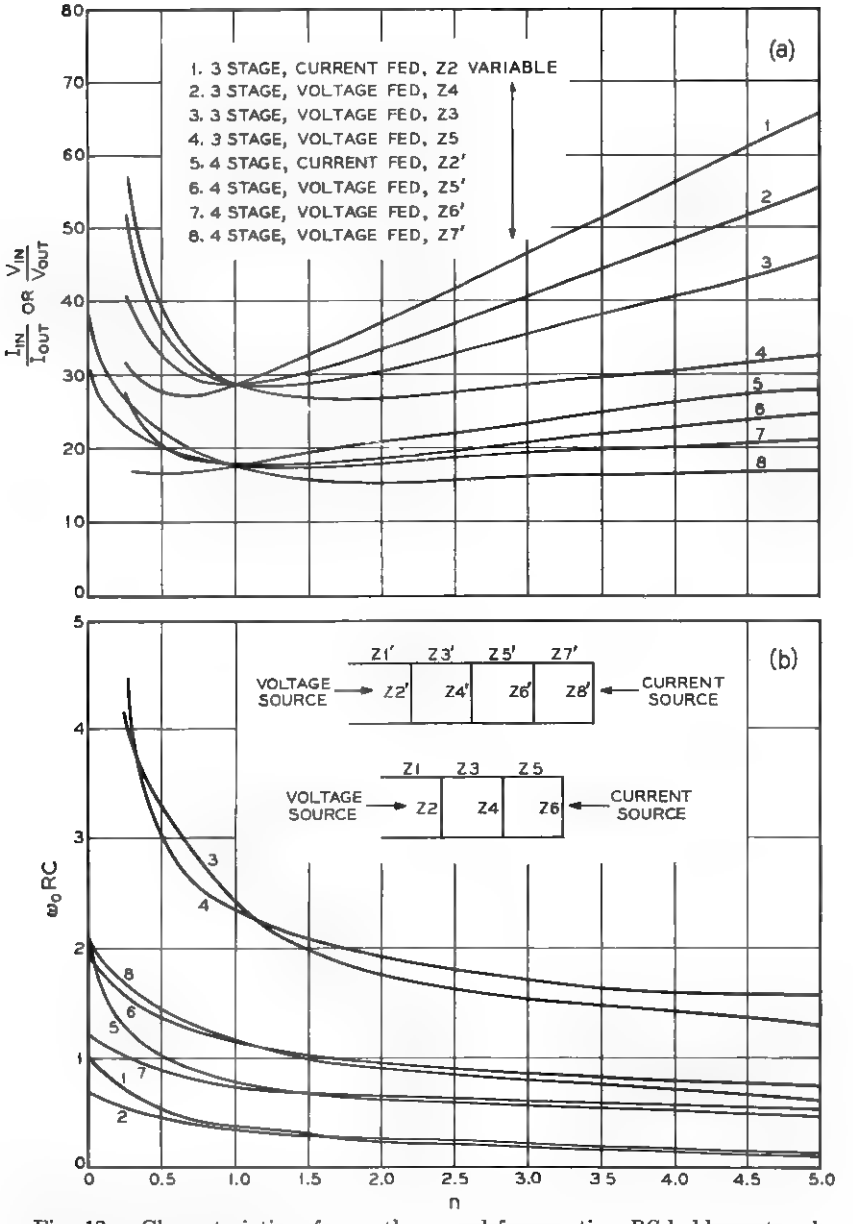

Fig. 12 — Characteristics of some three- and four-section *RC* ladder networks fed from a voltage or current source while varying a single ladder resistor. All *R*'s and *C*'s are equal except for the variable resistor $Z_i = nR$. All *R*'s are either in series or shunt, depending on the location of the respective Z_i: (a) attenuation versus *n*; (b) frequency versus *n*.

amplitude change was measured with up to 20 per cent frequency change. This range allows for modulation and initial tuning to be performed either by one and the same element or by two separate ones. If the amplifying section of the oscillator can be designed to be independent of transistor parameters and to have negligible phase shift at the frequencies in question, then the oscillator frequency is dependent only on the ladder network and control element. In the next section and the Appendix, the design of an *RC* 180° phase shift VCO utilizing these features is described in detail.

IV. RC FILTER AND FREQUENCY DISCRIMINATOR FOR THIN FILM DATA RECEIVER

In this section an application of the APLL as *RC* channel filter and frequency discriminator for a multichannel binary FM data receiver is described. The channel and frequency distribution of the transmitted data signal are shown in Fig. 13. Eight signal channels and one timing channel spaced evenly over a 1.43-kc frequency band are received simultaneously from the transmission line. Each channel is frequency modulated with a deviation of ±35 cps at a maximum rate of 75 bps. Adjacent channels are separated by a guard band of 100 cps.

The block diagram in Fig. 14(a) shows the circuits that are normally used in a receiver for this kind of binary FM data.[21] An AGC system is connected to the receiver input to compensate for losses suffered in the transmission line. Each channel has a bandpass filter and FM discriminator assigned to it. A post-detection filter follows to separate the actual data output from the higher-frequency detection products. It might also be used to give additional noise rejection and shaping in the baseband region. The filtered data signal drives a slicer whose output is

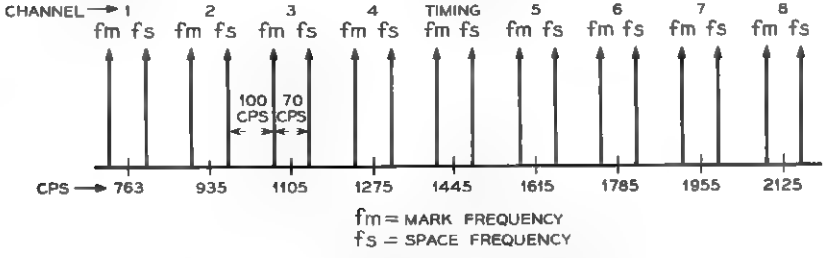

Fig. 13 — Frequency distribution of a multichannel data receiver.

sampled at appropriate instants by the timing channel to recover the binary data sequence. Fig. 14(b) shows the equivalent block diagram using the APLL. An APLL replaces the receiving bandpass filter and FM discriminator in every channel. Each APLL is followed by an *RC* active low-pass filter that serves the same purpose as the post-detection filter mentioned above. The transmitted binary data sequence can be obtained from a sampled slicer in the conventional way.

This particular transmission system was chosen because its very stringent filtering requirements are well suited to test the efficiency of *RC* active circuits that satisfy the restrictions imposed by microminiaturization techniques.

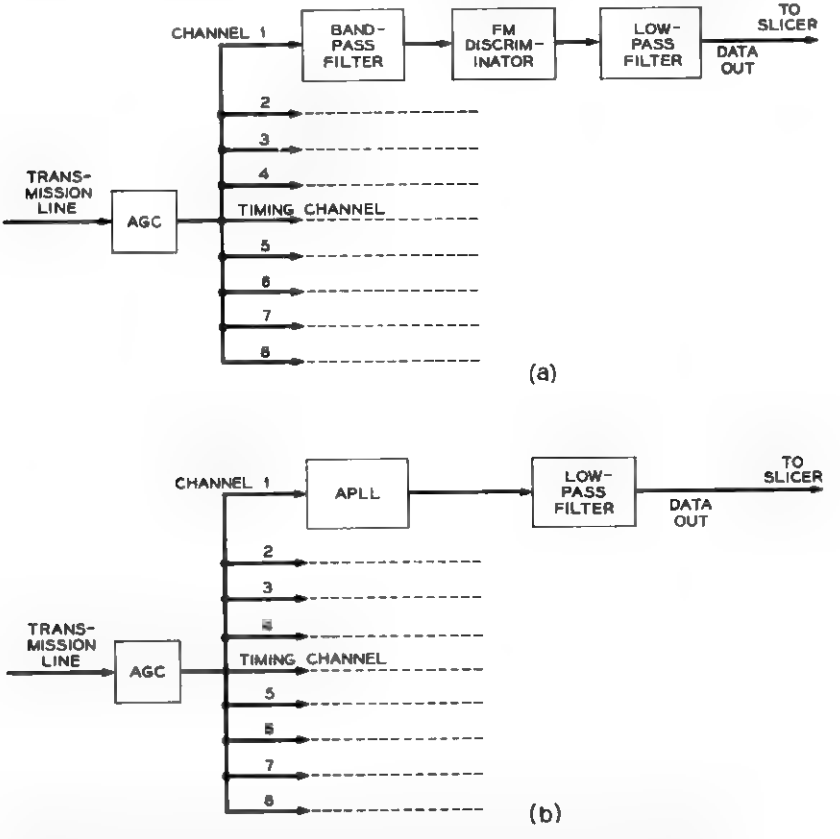

Fig. 14 — Block diagram of multichannel data receiver: (a) conventional circuits, (b) bandpass filters and FM discriminators replaced by APLL's.

4.1 *Design Requirements*

The miniaturization technique that has been chosen for these data sets combines tantalum thin film passive components with specially packaged active components.[22] The requirements that the circuits must then fulfill can be summarized as follows:

(a) for compatibility with thin film techniques:

no magnetic elements (inductors, transformers, etc.)

resistors not larger than 100 kilohms, not smaller than 100 ohms

high-quality capacitors not larger than 0.01μf; coupling capacitors not larger than 1μf

only one resistor adjustment at a time (by anodization); ease of tuning. This implies minimum interdependence between Q and frequency adjustments of a circuit.

(b) for stability, size reduction and economical compatibility:

circuit characteristics dependent only on passive components

as few components, in particular active ones, as possible.

4.2 *Loop Gain Requirements*

The over-all loop gain or lock range K is determined either by the linearity or capture frequency range, depending on the stability of the circuitry involved. High-stability tantalum thin film components are available for the application described here. The choice for high system stability and poor figure of merit F was therefore a natural one, so that the smallest loop gain compatible with loop linearity (35) was used.

Assuming a linearity error of approximately 10 per cent, the maximum phase error φ_{LIN} should not exceed $\pm 45°$. With an input frequency deviation of ± 35 cps the lock range is then given by:

$$K = 2\pi \times \sqrt{2} \times 35 \approx 2\pi \times 50 \text{ rad/sec.} \tag{40}$$

The distribution of gain within the loop is determined by the required discriminator output voltage for a specified frequency deviation at the input, in other words by the VCO sensitivity K_2. If the switched modulator cannot supply the remaining gain $K_1 = K/K_2$, a dc amplifier has to be incorporated in the system.

The discriminator output level was chosen at 4 volts peak-to-peak. Therefore

$$K_2 = \frac{2\pi \times 35}{2} = 110 \text{ rad/volts sec,} \tag{41}$$

and

$$K_1 = K/K_2 = 2.86 \text{ volts.} \tag{42}$$

The switched modulator output voltage (39) is maximum for equal ON/OFF switching times. With $R_S \ll R_L$ and E designating the amplitude of the input signal being filtered, (39) then simplifies to:

$$v_{out} = (E/\pi) \cos \varphi. \tag{43}$$

For n independent channels of equal average energy, the amplitude of a single-input signal in terms of the total rms input voltage $\overline{E_T}$ is given by:

$$E = (2/n)^{\frac{1}{2}}\overline{E_T} \tag{44}$$

which is approximately 0.35 v for each of the nine channels of the system here in question. The constant factor in (39) then equals 0.11 v. To satisfy (42), a dc amplifier with a voltage gain of 26 has to be added in the loop. An emitter-coupled differential dc amplifier was used for this purpose.

4.3 *Bandwidth Requirements*

For the data system considered here, optimum detection results when the receiving filter bandwidth is equal to the total frequency deviation in each channel. This corresponds to a bandwidth or crossover frequency of the open-loop gain (18) of ± 35 cycles. To minimize distortion caused by interference at the input, a system with minimum noise bandwidth is chosen. From (29) or Fig. 7, setting $\Delta\omega_{1c} = 35/50 = 0.7$, the relative system frequency

$$x = \omega_n/K = 0.77 \tag{45}$$

and with (27), the damping factor

$$\zeta_0 = 0.63. \tag{46}$$

τ_1 and τ_2 can now be calculated from (16) and (17). Referring to Fig. 2(b), with $R_2 = 5.1$ kilohms, R_1 and C follow from (15a) and (15b), giving 3 kilohms and 0.67 μf respectively.

The switched modulator is followed by a simple RC low-pass filter section that greatly attenuates the ac components of the error voltage before applying it to the dc amplifier. The ratio of channel frequency to system bandwidth is large enough to permit this without affecting the capture ratio (see Section 2.2). With the 3-db cutoff frequency

$\omega_{co} = 1.8K = 2\pi \times 90$ cps the fundamental frequency (i.e., twice the channel frequency) is attenuated by approximately 30 db in the lowest channel.

The baseband low-pass filter following the APLL is designed to reject the remaining high-frequency products, generated in the APLL by the switched modulator, while passing the data output with minimum attenuation. To obtain sufficient selectivity for this purpose an active low-pass filter with a cutoff frequency of 60 cps and a slope of 18 db/oct is used.

4.4 *Stability Requirements*

The maximum phase error $\varphi_{LIN} = \pm 45°$ that was used to derive the lock range given by (40) also defines the ratio of capture range to system bandwidth. From (36) we get:

$$F = \left(\frac{1}{\sin \varphi_{LIN}}\right)^{\frac{1}{2}} = (2)^{\frac{1}{2}} = 1.19 \tag{47}$$

which could have been obtained directly from Fig. 8. With the frequency deviation of ± 35 cps the capture range therefore extends over ± 42 cps. This allows for a drift in frequency of the APLL of ± 7 cps or 0.33 per cent at the highest channel (2125 cps). Designing the active circuitry of the APLL to depend solely on the high-precision thin film components, this stability can well be maintained. Initial tuning of the VCO (see Appendix) is accomplished by means of precision anodization of a resistor in the ladder network. This can be performed with up to 0.02 per cent accuracy.[23] Frequency stability is maintained by balancing the temperature coefficient of the capacitors by that of resistors. In this way the temperature coefficient of frequency can be held well under the permissible limit.

4.5 *Circuit Design*

The breadboard model of an APLL for one channel of the data receiver described above was built with conventional *RC* components. Channel center frequency was 1955 cps. A schematic of the circuit is shown in Fig. 15. High quality NPN Si planar epitaxial transistors and Si diffused-junction diodes were used throughout.

A 180° phase shift oscillator with one voltage-variable ladder element was used as VCO. This was quite adequate, as the maximum relative frequency deviation occurring at the lowest channel does not exceed 5 per cent. To insure linear operation of the voltage-variable element, it was inserted in a network section of low signal level. Since the attenua-

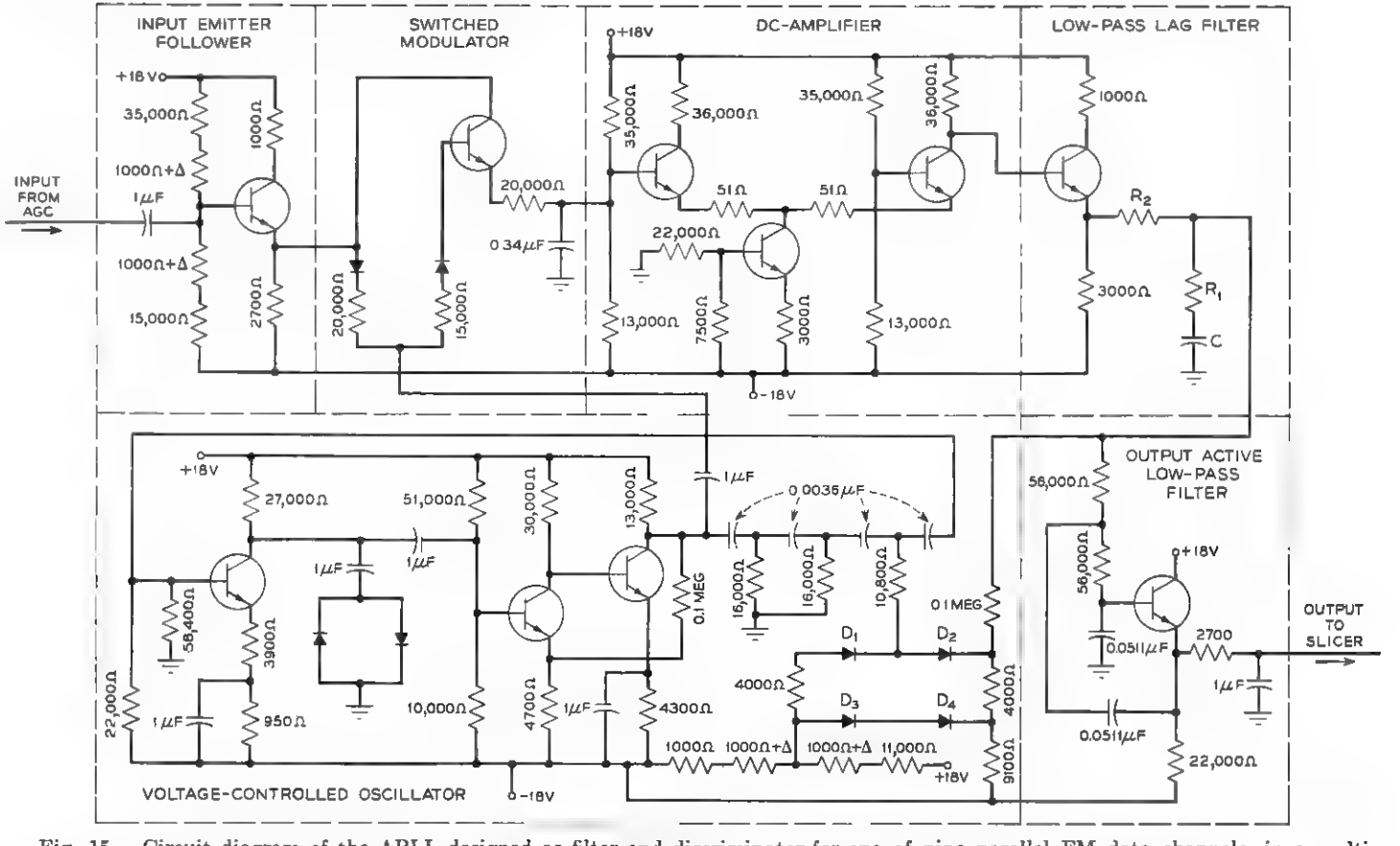

Fig. 15 — Circuit diagram of the APLL designed as filter and discriminator for one of nine parallel FM data channels, in a multichannel data receiver. All transistors are high-quality *NPN* Si planar-epitaxial, all diodes are Si diffused-junction types.

tion minimum is flatter for four- than for three-section ladder networks, while the difference in frequency sensitivity is not appreciable, the former configuration was used. The necessary gain is also lower for this configuration, allowing for sufficient current and voltage feedback to make the 3-stage voltage amplifier independent of transistor parameters. A varistor limits the oscillation amplitude, enabling the amplifier to be operated in its linear range. This improves temperature and voltage stability. It also eliminates signal distortion, so as to maintain constant switching intervals at the modulator.

The small-signal ac resistance of two forward-biased parallel silicon diodes was used as the voltage-variable shunt element in the ladder network. It is inversely proportional to the biasing current, if the semiconductor and lead resistance can be neglected. To reduce temperature variations, the diodes are biased by a constant current which is much larger than the leakage current. The frequency-voltage characteristic for small frequency deviations is derived in the Appendix.

A one-transistor switched modulator is used as multiplier. It is driven by the 15-vpp reference signal coming from the VCO. A preceding emitter follower feeds the composite signal into the APLL of each channel. The biasing voltage divider is adjusted for minimum voltage offset across the switched transistor. The simple *RC* low-pass filter mentioned in Section 4.3 connects the multiplier with an emitter-coupled dc amplifier.

The amplifier output is passed through a lag network and current controls diodes D_1 and D_2 in the oscillator. The initial steady-state biasing current in the diodes is set by a voltage divider. The diodes D_3 and D_4 serve to temperature stabilize the oscillator (see Appendix).

The discriminator output voltage is taken from the lag filter output terminal. To reject still remaining high-frequency components it is passed through an active low-pass filter before being further utilized.

4.6 *Experimental Results*

Measurements on the over-all performance of the APLL both as bandpass filter and discriminator and with respect to stability with temperature and voltage supply variations were made. The bandpass characteristic was measured while varying the bit rate of the incoming signal. One side of it is plotted in Fig. 16 in terms of the corresponding modulation frequency. It coincides well with the requirements listed in Section 4.3. The influence of the post-detection active low-pass filter

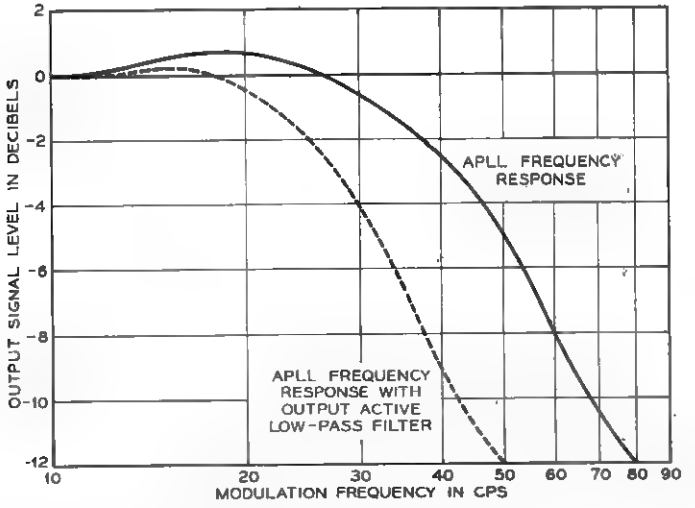

Fig. 16 — Measured frequency response of the APLL used as channel-filter and FM discriminator in a multichannel data receiver.

following the loop is illustrated in the same figure by the dashed curve. Fig. 17 shows waveforms for single- and multiple-channel inputs and for two different data speeds as they appear at the output of the post-detection filter. Fig. 18 shows the measured and calculated characteristics of the voltage-controlled oscillator used. It was built for a rest frequency of 1955 cps following the design procedure given in the Appendix. With the means of temperature compensation described there the relative frequency drift attained with conventional RC components was reduced to 0.25 per cent over a temperature range varying from 70°F to 140°F. Due to the amount of feedback possible in the three-stage amplifier section of the oscillator, the relative frequency change with ±2-v supply voltage variations was in the range of 0.1 per cent. The transistors of the dc differential amplifier were preselected and housed in a ten-lead TO-5 package. In this way the voltage drift with temperature variations was negligible.

Error rate measurements on the APLL designed as a combined filter and discriminator for one channel of the data receiver with different loop parameters have been performed. Further experimental and analytical work must, however, be completed before an evaluation of the error performance of the APLL or a comparison with conventional discriminators can be made.

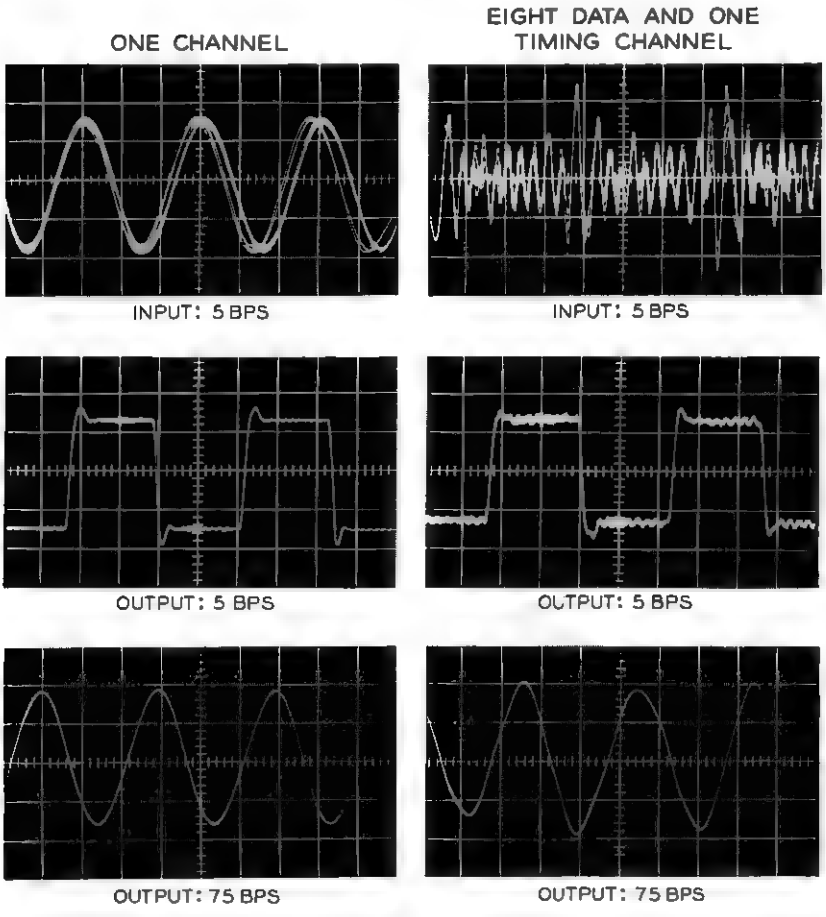

Fig. 17 — Output waveforms for single- and multiple-input signals and variable data speeds.

V. CONCLUSION

It has been shown that the APLL can be used as an FM signal separator and discriminator. Its signal separating properties allow for it to replace conventional bandpass filters in FM multiplex applications. The circuits entailed can be designed to satisfy the restrictions imposed by *RC* circuit miniaturization techniques. This makes it a useful device in the microminiaturization field, where practical solutions to the frequency selection problem are still few. Furthermore, it has the advantage

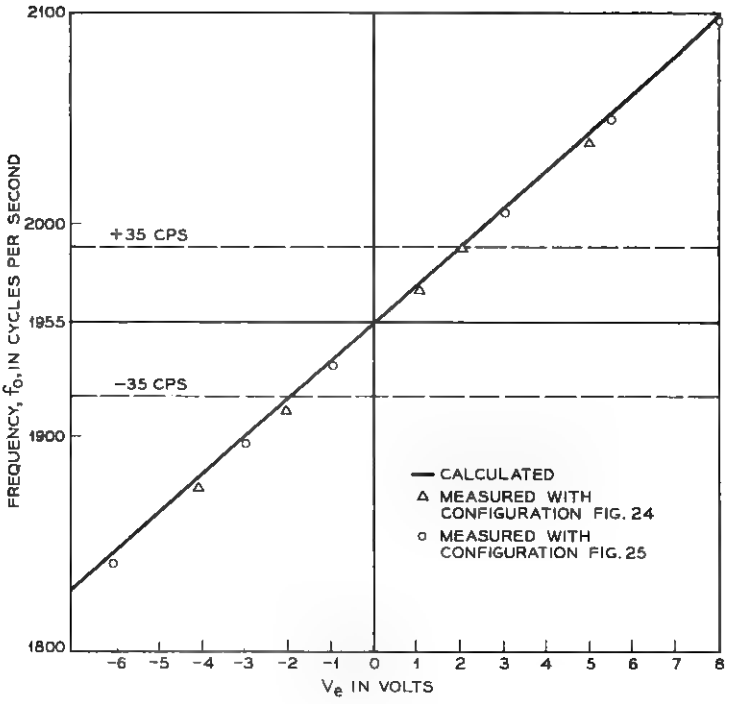

Fig. 18 – Oscillator frequency versus control voltage for the VCO shown in Fig. 12.

of ease of adjustment and reduction in circuit components over other comparable *RC* filtering methods.

In most applications the basic purpose of the APLL is to track narrow-band signals in a high-noise environment while maintaining minimum phase error. To do this the loop is designed so that the slowly varying frequency deviations to be tracked and the effective system bandwidth are very small with respect to the lock range. For this case the fact that the narrow bandwidth severely decreases the capture range is of no consequence.

For the type of application described in this paper, the system requirements of the APLL differ somewhat from those usually encountered. The limitations on phase error magnitude are given only by the requirement of linear loop action and are, therefore, not severe, i.e., the phase error may be as large as one radian. When the APLL is employed specifically as a digital data filter and demodulator the input frequency deviation is constant; for analog data applications the maximum devia-

tion must be given. The modulation frequency at the input may vary within a wide range, the only limit being given by the system bandwidth itself. The bandwidth of a given system cannot be arbitrarily reduced by low-pass filter modifications within the loop, because of the ensuing decrease in capture range. If, namely, the system is both to lock rapidly onto any initial frequency within the specified input frequency deviation as well as to relock rapidly after extraneous perturbations (e.g., impulse noise) might have thrown the system out of lock, the capture range has to cover the maximum frequency deviation. It is this last requirement that limits the attainable selectivity of a system all of whose parameters except those of the incorporated low-pass filter are given. An approximate expression relating system bandwidth and capture range has been derived for two types of low-pass filters. The minimum usable bandwidth compatible with a given frequency deviation thus results. It extends over a frequency band comparable to the capture range. Frequency deviation, minimum bandwidth, and capture range do not, therefore, differ greatly from one another.

As long as the lock range extends sufficiently beyond the maximum given frequency deviation, its value is not critical theoretically. Since it represents the total loop gain, however, it is uneconomical to make it larger than necessary. Its minimum value is determined by the requirement for linear loop operation. At the same time allowance must be made for a degree of circuit instability. This becomes increasingly important for narrow band systems operating at high channel frequencies. Using conventional circuit components and techniques the choice of lock range is therefore decided by the economics of designing for high circuit stability or for high loop gain. On the other hand with the major current microminiaturization techniques involving semiconductor integrated or thin film circuits the decision depends mainly on the inherent stability characteristics of the particular technique being used.

VI. ACKNOWLEDGMENT

The author would like to thank G. Malek for having carried out much of the laboratory work connected with the experimental results described in this paper.

APPENDIX

Analysis of 4-Section 180° Phase Shift Voltage-Controlled Oscillator with Single Variable Resistance

An equivalent diagram of the type of phase shift oscillator used is shown in Fig. 19. For an ideal voltage amplifier, $q = 0$, $m = 1$. The

variable element is nR. For no control voltage, the oscillator is at its rest frequency ω_c and $n = n_0$. The generalized oscillator frequency derived from Fig. 19 is given by:

$$\omega_0 = \frac{1}{RC}\left(\frac{2n + m + q + 4}{mn(q + 3) + n(5q + 4) + 3m(q + 1) + q}\right)^{\frac{1}{2}} \tag{47}$$

and the voltage gain necessary to compensate for network losses by:

$$-\frac{V_2}{V_1} = \frac{1}{mn\omega^4C^4R^4} - \frac{1}{\omega^2C^2R^2} \cdot\left[\frac{3(1 + q)}{mn} + \frac{7 + 2q}{m} + \frac{4 + q}{n} + 1\right] + q\left[\frac{1}{m} + \frac{1}{n} + 2\right] + 1. \tag{48}$$

Usually at least one of the two conditions for a perfect voltage amplifier can be fulfilled, sometimes at the cost of the other. Assuming for instance that the amplifier input impedance is much higher than the ladder shunt resistance ($m = 1$), (47) simplifies to:

$$\omega_0 = \frac{1}{RC}\left(\frac{2n + q + 5}{n(7 + 6q) + 4q + 3}\right)^{\frac{1}{2}}. \tag{49}$$

Substituting (49) in (48):

$$-\frac{V_2}{V_1} = \frac{1}{n}\left[\left(\frac{n(7 + 6q) + 4q + 3}{2n + q + 5}\right)^2 - \{n(8 + 2q) + 4q + 7\} \cdot\left\{\frac{n(7 + 6q) + 4q + 3}{2n + q + 5}\right\} + n(3q + 1) + q\right]. \tag{50}$$

Equations (49) and (50) have been plotted for different values of q in Figs. 20 and 21, respectively.

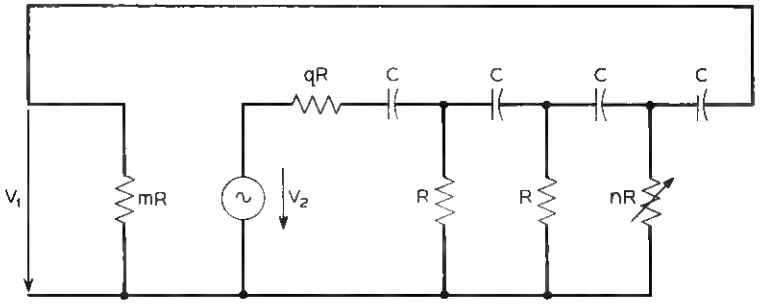

Fig. 19 — Equivalent diagram of a four section 180° phase shift audio oscillator with a single variable resistance, when fed from a nonideal voltage source.

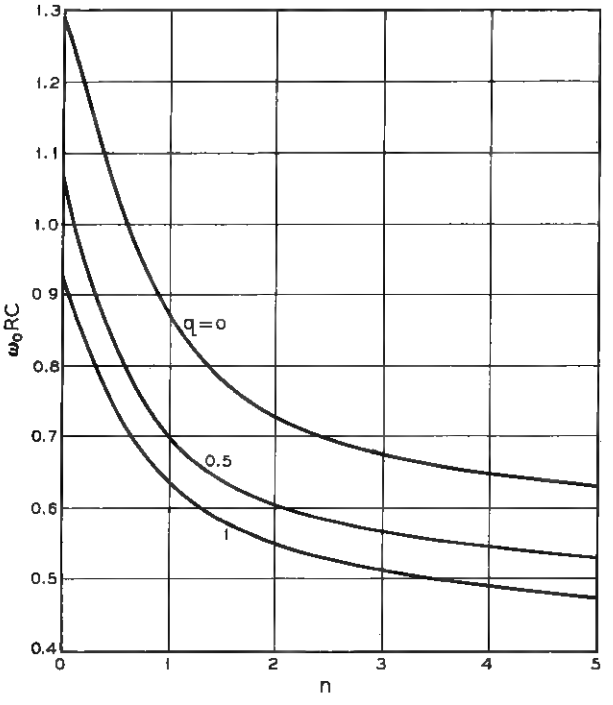

Fig. 20 — Frequency curves of a four-section ladder network with one variable resistor and the parameter q.

Fig. 21 shows that the point of minimum voltage loss does not occur when the ladder configuration is uniform. In the vicinity of the attenuation minimum, the curves are flat and it is possible over a given frequency range to choose a point n_0 for negligible voltage variation.

Expanding the frequency in a Taylor series around the rest frequency $\omega_c = \omega_0(n_0)$, (49) becomes:

$$\omega_0(n) = f(n)$$

$$= f(n_0) + \frac{df(n_0)}{dn}\frac{(n - n_0)}{1!} + \frac{d^2f(n_0)}{dn^2}\frac{(n - n_0)^2}{2!} + \cdots. \tag{51}$$

Retaining only the first two terms of the series, whereby

$$\omega_c = \frac{1}{RC}\left(\frac{2n_0 + q + 5}{n_0(7 + 6q) + 4q + 3}\right)^{\frac{1}{2}} \tag{52}$$

and

$$\nu = -\frac{\omega_c}{2}\frac{6q^2 + 29q + 29}{(2n_0 + q + 5)[n_0(7 + 6q) + 4q + 3]} \text{ rad/sec} \quad (53)$$

(51) becomes:

$$\omega_0(n) = \omega_c + \nu(n - n_0). \quad (54)$$

A voltage-dependent shunt element consisting of a combination of current-driven silicon diodes, a resistor and a capacitor is shown in Fig. 22. The diodes are dc-biased in series, but due to the large capacitor shunting them are ac-connected in parallel. The resulting symmetrical ac resistance seen from the ladder network reduces distortion that might arise from nonlinear operation of the diodes if the signal level is not sufficiently small. To keep the level as small as possible, this configura-

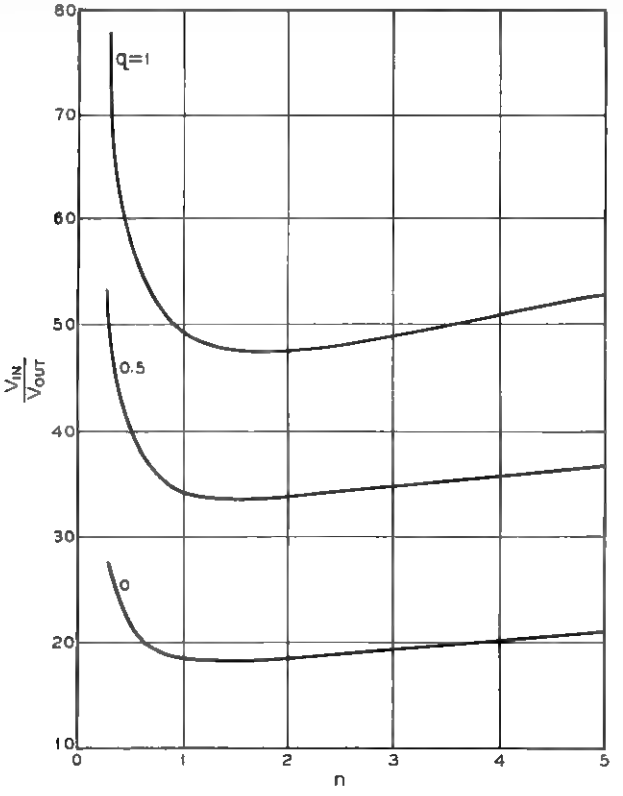

Fig. 21 — Attenuation curves of a four-section ladder network with one variable resistor and the parameter q (see text).

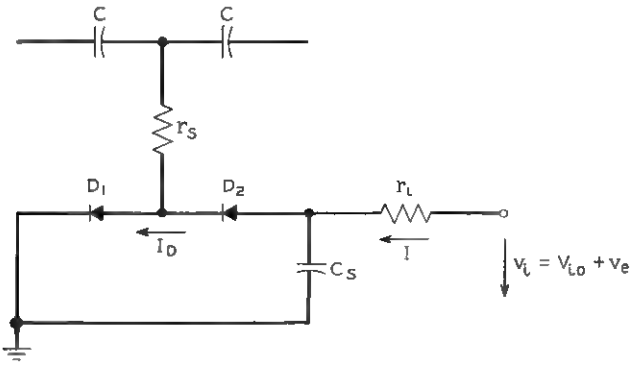

Fig. 22 — Voltage variable, ladder shunt resistance using diodes.

tion substitutes the third shunt element of the ladder network. The fourth is reserved as a voltage divider to bias the first amplifier stage of the oscillator.

The incremental ac resistance of an ideal forward-biased diode is given by:

$$r_D = \frac{kT}{e} \frac{1}{I_D + I_0} \tag{55}$$

where the familiar term kT/e equals 25 millivolts at room temperature. I_D and I_0 denote the forward biasing and leakage currents, respectively. Silicon diodes are used, which have very small leakage currents, so that $I_D \gg I_0$ and

$$r_D \approx \frac{kT}{e} \frac{1}{I_D} = \frac{V_0}{I_D}. \tag{56}$$

The small-signal resistance is therefore inversely proportional to the diode current.

Fig. 23 shows the measured small-signal conductance of two silicon diodes of the type used in a configuration as shown in Fig. 22. The curve extends linearly over a wide range as theoretically predicted. Furthermore, measurements with numerous silicon diodes were very consistent. Because no account is taken of the lead and semiconductor resistance of the diode, nor of surface leakage effects, a steeper slope would, however, be expected. Nevertheless, since the modified diode configurations actually used reduce the influence of the diode charac-

teristics, the resulting VCO performance can be predicted sufficiently accurately.

It can be shown[24] that r_D is considerably less dependent on temperature change when fed from a current rather than from a voltage source. If necessary, additional temperature compensation is easily effected for current-fed diodes, as will be shown later.

Referring to Fig. 22, it is now of interest to calculate the change in oscillator frequency caused by the control voltage deviation v_e. To do so, the Taylor series (51) can be expanded around the steady-state diode current I_{D0} corresponding to the steady-state control voltage V_{i0} and to the oscillator rest frequency ω_c. With the results already obtained in (54) and referring to Fig. 22, the first two terms of (51) then become:

$$\omega(v_i) = \omega_c - \nu \frac{dn}{dI_D}(I_{L0}) \frac{dI_D}{dv_i}(I_{D0})v_e \tag{57}$$

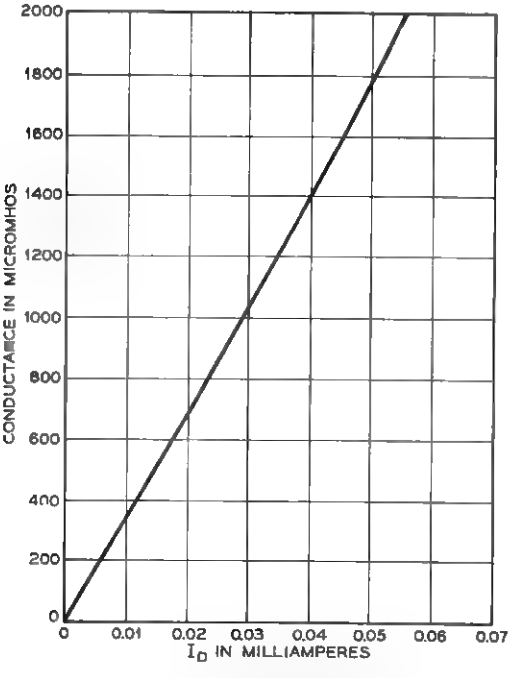

Fig. 23 - Small-signal conductance of two silicon diodes versus biasing current in the configuration shown in Fig. 22.

where

$$v_i = V_{i0} + v_e$$

and V_{i0} is the steady-state component of the control voltage and v_e its voltage increment. With the substitutions

$$\epsilon(I_D) = dn/dI_D \tag{58}$$

$$\kappa(I_D) = dI_D/dv_i \tag{59}$$

(57) becomes:

$$\omega(v_i) = \omega_c - \nu\epsilon\kappa v_e . \tag{60}$$

Comparing Figs. 19 and 22,

$$nR = r_s + \frac{1}{2}\frac{V_0}{I_D} \tag{61}$$

so that:

$$\epsilon(I_{L0}) = -\frac{1}{2R}\frac{V_0}{I_{D0}^2}. \tag{62}$$

From inspection of Fig. 22, we may write:

$$v_i = r_i I + 2V_D \tag{63}$$

and

$$I = I_D \tag{64}$$

where V_D is the voltage across one of the diodes. Assuming idealized diodes with negligible lead resistance:

$$V_D = V_0 \ln\left(\frac{I_D}{I_0} + 1\right). \tag{65}$$

Combining (63), (64) and (65) and differentiating with respect to the input voltage v_i,

$$\kappa(I_{L0}) = \frac{I_{L0}}{r_i I_{D0} + 2V_0}. \tag{66}$$

In (60) ν is determined by the oscillator frequency ω_c, the optimum choice of n_0, and the ratio of amplifier output to ladder resistance q. To insure current biasing of the diodes, r_i is limited in size either by the values attainable with thin film technology or by the output capa-

bilities of the preceding dc amplifier. This leaves the diode current I_{D0} to be chosen appropriately for a specified VCO sensitivity K_2. Since

$$K_2 = \nu\epsilon\kappa \tag{67}$$

it follows from (62) and (66) that:

$$I_{D0} = \left(\frac{V_0^2}{r_i^2} + \frac{\nu}{2K_2}\frac{V_0}{Rr_i}\right)^{\frac{1}{2}} - V_0/r_i. \tag{68}$$

As would be expected from the forward-biased diode characteristic or from Fig. 23, the current operating point decreases with an increase in the specified VCO sensitivity K_2.

The remaining network parameter r_s can now be determined by satisfying the condition that $n = n_0$ when $I_D = I_{D0}$. From (61)

$$r_s = n_0 R - \frac{1}{2}\frac{V_0}{I_{D0}}. \tag{69}$$

The frequency characteristic of the VCO incorporating the network shown in Fig. 22 and given by (53), (60), (62) and (67) is linear only over very small voltage increments. This is due to the nonlinear diode characteristics. Linearity can be greatly improved by modifying the voltage variable network according to Fig. 24. The additional resistor r_p shunting the diodes reduces κ and with it the influence of the nonlinear diode characteristics. Going through the same derivations as above

$$\kappa(I_{L0}) = \frac{r_p}{r_i + r_p}\frac{I_{D0}}{\frac{r_i r_p}{r_i + r_p} I_{D0} + 2V_0} \tag{70}$$

while ν and ϵ remain unchanged. This simplifies to

$$\kappa(I_{L0}) \approx \frac{r_p}{r_i}\frac{I_{D0}}{r_p I_{D0} + 2V_0} \tag{71}$$

if $r_i \gg r_p$.

A value of r_p can now be chosen such that r_i is at least an order of magnitude larger. The diode current necessary to establish a specified VCO sensitivity K_2 then follows from (62) and (70), namely:

$$I_{D0} = \left[\left(\frac{V_0}{r_p'}\right)^2 + \frac{\nu V_0}{2K_2 R r_i}\right]^{\frac{1}{2}} - \frac{V_0}{r_p'} \tag{72}$$

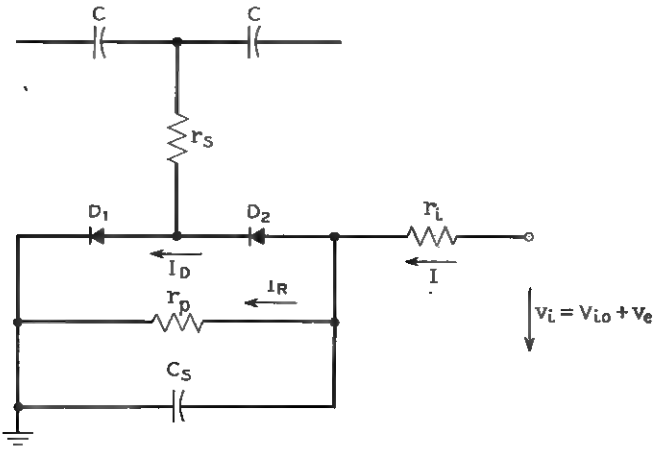

Fig. 24 — Modification of Fig. 22.

where

$$r_p' = \frac{r_p r_i}{r_p + r_i}. \tag{73}$$

Since $r_i \gg r_p$

$$I_{D0} \approx \left[\left(\frac{V_0}{r_p}\right)^2 + \frac{\nu V_0}{2K_2 R r_i}\right]^{\frac{1}{2}} - \frac{V_0}{r_p}. \tag{74}$$

It is apparent again here that I_{D0} increases with reduced VCO sensitivity K_2.

As in the preceding case, the remaining resistor r_s can now be determined by comparison of Figs. 19 and 24. The same value as before, given by (69), is found.

The characteristics of the low-pass filter consisting of r_i and C_s in the diode configuration of Fig. 24 will interfere with the operation of the APLL if its 3-db cutoff frequency cannot be maintained higher than the lock range of the loop (see Section II of main text). If this is the case the configuration shown in Fig. 25 must be used. If r_i is sufficiently larger than r_{p1} and r_{p2}, the latter two resistors can be made equal. Derived in the same manner as before,

$$\kappa(I_{D0}) = \frac{r_p}{r_i + r_p} \frac{I_{D0}}{\frac{r_p}{r_i} + r_p(2r_i + r_p)I_{D0} + 2V_0} \tag{75}$$

where again ν and ϵ remain unchanged. If $r_i \gg r_p$

$$\kappa(I_{L0}) \approx \frac{1}{2}\frac{r_p}{r_i}\frac{I_{D0}}{r_p I_{D0} + V_0}. \tag{76}$$

With the choice of r_p at least an order of magnitude smaller than r_i and substituting (62) into (75)

$$I_{L0} = \left\{V_0^2\left[\frac{r_i + r_p}{r_p(2r_i + r_p)}\right]^2 + \frac{\nu V_0}{2K_2R(2r_i + r_p)}\right\}^{\frac{1}{2}} - V_0\left[\frac{r_i + r_p}{r_p(2r_i + r_p)}\right]. \tag{77}$$

With $r_i \gg r_p$

$$I_{D0} \approx \left[\left(\frac{V_0}{2r_p}\right)^2 + \frac{\nu V_0}{4K_2Rr_i}\right]^{\frac{1}{2}} - \frac{V_0}{2r_p}. \tag{78}$$

From a comparison of Figs. 19 and 24

$$r_s = n_0R - \frac{r_p}{2} - \frac{V_0}{2}\frac{1}{I_{D0}}. \tag{79}$$

Eliminating the diode current from (78) and (79), a simplified expression relating r_p with r_s results, namely:

$$r_s \approx R\left(n_0 - \frac{r_p}{2R}\right) \tag{80}$$

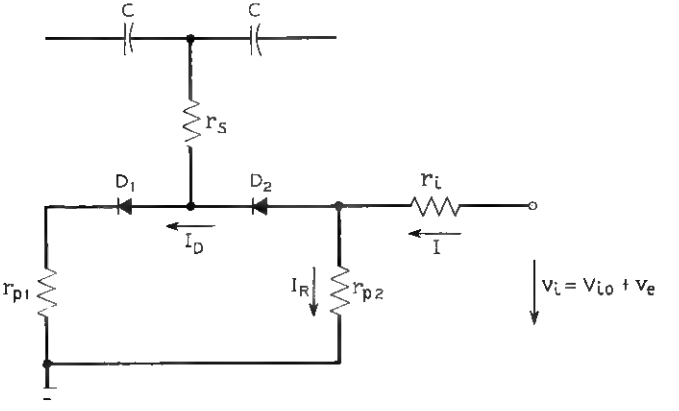

Fig. 25 - Another modification of Fig. 22.

when the specified VCO sensitivity

$$K_2 \ll \frac{r_p}{r_i} \frac{\nu}{V_0}.$$

The oscillator design can now proceed as follows: R is chosen such that with the largest available high-precision thin film capacitors (0.01 μf) the lowest necessary oscillator frequency can be obtained (in the data receiver described in the text, this corresponds to the lowest channel frequency). For all higher frequencies only the ladder capacitors are changed. If the capacitor value is not critical, R is chosen to conform with amplifier biasing considerations and to minimize q. q is given by the ratio of amplifier output impedance to R. n_0 is chosen for minimum voltage loss over a given frequency range and is obtained from Fig. 21. C results from (52) for a given frequency ω_c. ν is obtained from (53). The largest value of r_i compatible with thin film techniques and the output capabilities of the preceding stage is chosen, and r_p is made at least an order of magnitude smaller. The steady-state diode current is then given by one of the appropriate equations above, using the desired VCO frequency-voltage slope K_2. To obtain oscillation at the desired rest frequency, r_s is then determined by the appropriate expression derived above.

At this point a word must be said about the accuracy of (47) or (52) in connection with thin film tuning techniques. (47 might just as well have been used for the above computations, but would have been somewhat cumbersome.) In spite of the input and output impedances of the oscillator being taken into account, the frequency of the actual circuit may be lower than the predicted value owing to coupling, blocking and stray capacitance in the amplifier section not taken into account by the calculations. Initial oscillator frequency adjustment is therefore imperative. Thin film resistor adjustments can be made either by additional anodizing of the resistor films or by scratch-pad techniques in which the sides of thin film lattice configurations are progressively opened mechanically. Both methods are irreversible and only increase resistor values. To accommodate this circuit peculiarity, a frequency approximately 10 per cent higher than required is substituted in the equations defining the ladder capacitor C. In doing so n_0 is assumed equal to unity. Tuning the oscillator now consists of increasing the ladder resistance r_s (see Figs. 22, 24 and 25) and with it n_0, until the required frequency is reached. The necessary increase of n_0 can be computed from (54) and is approximately 25 per cent. Fortunately, this coincides with the region of minimum loss shown in Fig. 21. However, since the

attenuation curve is relatively flat for values of n larger than unity the exact value of initial frequency offset is not critical.

When biasing diodes from a constant-current source such that the leakage current is negligibly small, only the increase with temperature of $V_0 = kT/e$ has to be compensated for. The increase of this voltage has the over-all effect of increasing the oscillator frequency. By inserting two forward-biased silicon diodes in series with r_{p2} (see Fig. 25), the relative frequency variation is reduced to 0.25 per cent when the ambient temperature is varied from 70°F to 140°F. Due to the amount of feedback possible in the three-stage amplifier section of the oscillator, (see Fig. 15) the relative frequency change with ±2-v supply voltage variations is in the range of 0.1 per cent.

GLOSSARY

A: amplitude of VCO output

B: noise bandwidth of APLL

C: capacitance in uniform RC ladder network of 180° phase shift VCO

C_s: capacitance shunting diodes in VCO voltage variable network defined in Appendix

E: amplitude of single-channel input signal

E_c: amplitude of voltage controlling the switched modulator

$\overline{E_T}$: total rms voltage at APLL input

F: APLL figure of merit: capture range/3-db closed-loop bandwidth

F_0: APLL figure of merit: capture range/minimum-noise bandwidth

$F(j\omega)$: transfer function of low-pass filter

F_ω: amplitude-vs-frequency response of low-pass filter

$F_{\Delta\omega_i}$: filter frequency response at input frequency $\Delta\omega_i$

$F_{\Delta\omega_{ic}}$: filter frequency response at capture frequency $\Delta\omega_{ic}$

$f(t)$: impulse response of low-pass filter

Δf_i: maximum initial frequency offset before ultimate locking by APLL

I: input control current of VCO

I_D: diode bias current

I_{D0}: steady-state diode bias current

I_0: diode leakage current

I_R: current through resistance parallel with diodes in VCO voltage variable network defined in Appendix

K_1 : gain of phase detector and dc amplifier in volts

K_2 : gain (voltage sensitivity) of VCO in radians/(sec, volts)

$\pm K = K_1K_2$: steady-state loop gain and lock range of APLL in rad/sec

m: ratio of amplifier input impedance to ladder resistance R in 180° phase shift VCO

n: ratio of variable resistance to ladder resistance R in 180° phase shift VCO

n_0 : ratio of variable resistance to ladder resistance R at VCO rest frequency

q: ratio of amplifier output impedance to ladder resistance R in 180° phase shift VCO

R: resistance in uniform RC ladder network of 180° phase shift VCO

r_D : incremental ac resistance of ideal forward-biased diode

$r_{p1}, r_{p2}, r_p, r_s, r_i$: resistors in diode configurations dealt with and defined in Appendix

T: period of VCO output frequency

T_b : period of beat frequency ω_b

T_c : capture time, i.e., time it takes APLL to lock onto input frequency

T_{co} : time constant of simple RC low-pass filter

T_0 : switching time of switched modulator

$T(j\omega)$: discriminator transfer function of APLL

V_{io} : dc component of VCO control voltage v_i

$V_0 = kT/e$: where k is Boltzmann's constant, e the charge of an electron and T the temperature in degrees Kelvin

v_e : increment of VCO control voltage (error voltage) and discriminator output

v_{ec} : error voltage at capture instant

$\hat{v}_{ec}$: amplitude of error voltage at capture instant

v_i : control voltage of VCO

v_{out} : dc component of switched modulator output voltage

x: ratio of APLL undamped natural frequency ω_n to lock range K

$\epsilon = dn/dI_D$: sensitivity of resistance ratio n to incremental change in diode current for diode configuration dealt with in Appendix

ζ: ratio of actual to critical damping of APLL

ζ_0 : damping ratio for system with minimized noise bandwidth

$\kappa = dI_D/dv_i$: sensitivity of diode current to incremental change in control voltage for diode configurations dealt with in Appendix

μ: dc amplifier gain

$\nu = d\omega/dn$: sensitivity of VCO frequency to incremental change in n

τ_1, τ_2: time constants of low-pass lag network defined in Fig. 2(b)

$\varphi(t)$: instantaneous difference (error) between input and VCO phase

φ_e: phase error at capture instant

$\varphi_i(t)$: instantaneous input phase

φ_{LIN}: maximum phase error corresponding to given percentage linearity error in phase detector output characteristic

$\varphi_0(t)$: instantaneous VCO phase

$\psi(\omega)$: phase versus frequency response of low-pass filter

ω_b: out-of-lock beat between input and VCO frequency

ω_c: channel center frequency; VCO rest frequency

ω_{co}: 3-db cutoff frequency of simple RC low-pass filter

$\omega_i(t)$: instantaneous frequency of APLL input signal

ω_n: undamped natural frequency of APLL

$\omega_0(t)$: instantaneous VCO frequency

$\Delta\omega(t)$: difference between instantaneous input and VCO frequency

$\Delta\omega_1(t)$: instantaneous input frequency deviation from ω_c

$\Delta\omega_{ic}$: first approximation of capture frequency deviation at input and 3-db closed-loop bandwidth of APLL

$\Delta\omega_{ic}'$: closer approximation of capture frequency than $\Delta\omega_{ic}$

$\Delta\omega_0(t)$: instantaneous VCO frequency deviation from ω_c

$\overline{\Delta\omega_0}$: mean VCO frequency in the unlocked state

$\Delta\omega_{oc}$: first approximation of VCO capture frequency deviation; by definition $\Delta\omega_{ic} \equiv \Delta\omega_{oc}$

$\Delta\omega_{ic}/K$: first approximation of capture ratio, defined as ratio of capture-to-lock range

$\Delta\omega_{ic}'/K$: closer approximation of capture ratio than $\Delta\omega_{ic}/K$.

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